INVESTIGATION OF SILICON-ON-INSULATOR MATERIALS AND DEVICES FOR VLSI AND SPECIAL-DEVICE APPLICATIONS

BY

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TABLE OF CONTENTS

Abstract of Dissertation Presented to the Graduate School
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This work deals with the characterization, modeling, and design considerations of silicon-on-insulator (SOI) materials and devices for VLSI and special-device applications. It consists of two parts. In the first part, several electrical characterization techniques are described that use test structures such as diode, capacitor, and MOSFET for evaluating the film and interface properties of SOI materials and devices. In the second part, design considerations for enhancing the production yield in SOI VLSI circuits are discussed.

Using the SOI diode as a test vehicle, we develop a differential technique that uses the reverse biased current-voltage and capacitance-voltage measurements for determining the generation lifetime profile in the thin semiconductor film. To evaluate the top silicon film and the interface properties of the SOI substrate, we develop a generalized model for electrical characterization of a semiconductor-insulator-semiconductor (SIS) capacitor using static, dynamic, and transient capacitance and

conductance methods. By introducing a coupling factor, the conventional metal-oxide-semiconductor capacitor theory is modified and applied to analyze the properties of two Si/SiO_2 interfaces (i.e., film/buried oxide and substrate/buried oxide interfaces) of a SIS capacitor. In addition, we have also developed several methods for the characterization of interface states in a small geometry MOSFET operating in the linear region. Interface state densities determined by the high- and low-frequency transconductance measurements for both bulk and SOI MOSFETs are presented.

The production yield of VLSI circuits is investigated by examining the statistical variation of the threshold voltage induced by random distributed device parameters. The analysis reveals that thin-film SOI MOSFET is less sensitive to inherent fluctuations in device parameters. Design considerations in minimizing the statistical threshold voltage variation in SOI MOSFETs are discussed. By properly choosing the gate material, film thickness, and channel doping density, enhancement of production yield can be expected for high performance SOI VLSI circuits.

CHAPTER 1
INTRODUCTION

1.1 Silicon-On-Insulator Technology

The silicon-on-insulator (SOI) technologies have been under rapid development in the past few years. The SIMOX-based (Separation by IMplantation of OXygen) SOI material offers new promise as leading technology for high-density, radiation-hard, and high-performance integrated circuits (ICs). The useful SOI properties are based on the unique capability of total electrical isolation of silicon areas and the reduction of junction areas. The potential advantages of SOI technology over bulk silicon for advanced MOS devices are numerous. They include higher speed, lower dynamic power consumption, greater packing density, increased transient radiation tolerance, integration of bipolar and CMOS devices on the same chip, and, for CMOS, freedom from latch up.

High quality SOI material is required in order to achieve the potential for this technique in IC fabrication. There are several methods for making SOI layers, but, at present, three techniques are generally believed to hold the most promise. These are (i) ion implantation of oxygen below the silicon surface, (ii) recrystallization of polysilicon deposited on a thermally grown oxide, and (iii) wafer bonding. The use of a high-dose oxygen ion implantation, commonly known as SIMOX, is one of the major contenders for SOI technology. SIMOX wafer, unlike other SOI wafers, has the advantage that the material formation is simply an additional step in an IC fabrication process – ion implantation, furnace annealing, and epitaxial growth. It is a conventional silicon-based technology, and the fabrication of SIMOX-based

circuits uses processing steps similar to those used in the conventional IC manufacturing. Although research continues on both SIMOX and recrystallization-based SOI, SIMOX appears to be more compatible with conventional IC fabrication processes than recrystallization-based SOI. Therefore, SIMOX has been more heavily investigated and developed than the rest of SOI technologies.

1.2 Preparation of SIMOX Wafers

A SIMOX wafer is prepared by implanting a silicon wafer with oxygen ions at 150-200 keV and to an ion dose of typically 1.2-2.4 $\times$ $10^{18}/cm^2$ (Fig. 1.1). The dose used for this process is about 100 times larger than any other implant dose used in semiconductor processing. This dose translates into a very long implant time. Even with the highest-current implanter, which delivers 100 mA of beam current, the oxygen implant requires about 6-7 hours to implant twenty-five 4" wafers [1]. The temperature during implant is very important since in situ dynamic annealing must occur at the surface of the wafer. The wafer is typically heated to 400°C or higher during the ion implantation process. A high wafer temperature ensures that the film retains its crystallinity during the high-dose implantation process [2].

With such an extreme implant situation, several other matters become important. One is the metallic contamination introduced during the implant. Since oxygen ions are very reactive, structures inside the implanter that can be exposed to the ionized oxygen must be passivated, usually by coating with quartz or silicon. Nevertheless, some metallic contamination is present with all implanters, but the dose and current are usually much smaller, and the contamination tends to scale with dose. Early SIMOX wafer was found to have very high density ($1 \times 10^{17}/cm^3$) of the components of stainless, copper, carbon, and aluminum. The contamination has been reduced about two orders of magnitude by careful contamination control in the later version of the oxygen implant system [1].

After oxygen implantation, the wafer is typically annealed above 1150°C in an inert ambient. The high-temperature anneal repairs the damage introduced during implantation and allows excess oxygen in the surface silicon layer to out-diffuse, increasing the dielectric strength of the buried oxide layer. After implantation and anneal, the surface silicon layer is typically 100-300 nm thick. If a thicker silicon layer is required for IC fabrication, an epitaxial layer can be grown by conventional epitaxial techniques.

The two types of defects which are dominant in the top silicon film followed the high-temperature annealing are precipitates and threading dislocations. Although precipitates can be easily removed by dissolution during high-temperature annealing, the threading dislocations once formed are exceedingly stable and are essentially impossible to remove by thermal annealing alone [3]. Two different approaches can be identified to avoid the generation of threading dislocations during annealing: (i) sequential implantation and annealing of substoichiometric doses of oxygen, which has been found to be effective in reducing the dislocation density by limiting the maximum precipitate size attained during the early stages of annealing [4], and (ii) formation of a band of ordered oxide precipitates to reduce the stress in this region and to confine the dislocations to a narrow region above the buried oxide so that they can be removed as the precipitates are incorporated into the buried oxide [5].

Most of the implanted insulator layers are formed by oxygen implantation, however it is also possible to create a buried insulator layer by implanting nitrogen. Nitrogen has the advantage in that a lower dose is required to create the insulator, so that the silicon film will be damaged less. The competing effects that make the implanted nitrogen approach more difficult include a narrow window of doses that are useful and possible adverse effects of residual nitrogen in the silicon layer [1]. A very attractive approach is the use of both oxygen and nitrogen implants to form a buried oxynitride.

1.3 Integrated Circuit and Novel-Device Applications

Although CMOS remains the most dominant field of application for SOI technology, the ease of processing SOI substrates, the full dielectric isolation of the devices, and the possibility of using a back-gate have sparked a large research activity in the field of novel SOI devices. The immediate application of SOI technology is in radiation-hardened ICs for space and military applications. SIMOX is also useful for device isolation in the integration of low-voltage control circuits with high-voltage devices in power IC and telecommunication IC applications. Moreover, SIMOX is a potential asset for CMOS applications as device feature sizes below the 0.8 μm barrier. It is also a natural candidate for integration of bipolar and CMOS devices on the same chip and may allow the fabrication of the next generation high-density horizontal complementary bipolar devices.

1.3.1 Military Integrated Circuit Applications

Military ICs are required to operate at high speed and low power and be radiation-hardened and reliable under harsh environments. These circuits must operate reliably over a wide temperature range. SIMOX-based ICs address these needs. The superior radiation hardness of SIMOX ICs against total gamma dose and single-event upsets have clearly been demonstrated [6,7]. The hardness of SIMOX MOS devices is partly dependent on the interface between the device and the underlying oxide dielectric layer (film/oxide interface). A major strength of SIMOX is that the gamma-total-dose properties of the film/oxide interface can be improved by using different variations of the basic SIMOX formation process. Furthermore, the hardness of the film/oxide interface under radiation can be drastically improved by applying a small bias of less than -5 V at the substrate during irradiation [8].

Since SOI ICs are dielectrically isolated, little parasitic coupling exists between neighboring devices, and thus no latch-up is expected. This is very attractive for high-reliability IC applications under transient radiation, transient power surge, and

high-temperature environments that can readily cause latch-up in bulk-type circuits. With increasing ambient temperature, the standby power of a bulk-type IC increases due to increased junction leakage. However, in SOI ICs, where source/drain junctions are terminated by the buried oxide layer, standby power increases more slowly with increasing temperature because of the significantly reduced junction areas [9,10].

1.3.2 High-Voltage Integrated Circuit Applications

This type of ICs can be divided into two categories: (i) telecommunication ICs, which are required to handle high voltages but relatively low power levels; and (ii) power ICs, which are required to handle both high voltages and high power levels. With the continued scaling of device feature sizes and the continued desire to integrate more functions onto a monolithic chip, the isolation between adjacent devices is becoming a severe problem. Because of a variety of devices built on the same chip, optimizing their performance requires very complex processing for bulk silicon technology. Using SIMOX technology, the problem of device isolation is eliminated, making the design and manufacturing of monolithic high-voltage and power ICs a simpler task.

SOI-based power integrated circuits are dielectrically isolated from each other and, thus, intrinsically suited for high-voltage applications. An electric field shielding layer (EFS), a unique feature of SIMOX, provides SIMOX-based devices with a particular advantage for high voltage applications. An EFS layer increases the voltage that can be sustained across a particular device by a factor of 2 or more [11]. By incorporating a low-voltage with a high-voltage CMOS process on SIMOX, an advanced telecommunication IC has been fabricated [11]. The ease of incorporating high-voltage devices with low-voltage devices is further demonstrated by the fabrication of a lateral conductivity-modulated FET (COMFET) using a modified low-voltage CMOS process on SIMOX [12]. SIMOX technology also allows the fabrication of new power device structures such as the j-MOS [13]. The device is a potentially useful normally

on, low-voltage (less than 100 V) power switch.

1.3.3 Submicron CMOS Applications

Technological barriers are enormous when the feature size of CMOS devices is scaled below 0.8 μm. LOCOS (local oxidation of silicon) isolation will no longer be usable, and no workable alternative has yet been developed. The sharp roll-off of threshold voltage with reduction in gate length (a short channel effect) will cause severe yield loss unless very tight manufacturing tolerance can be achieved. Hot electron effect also places a severe limit on device design and on gate oxide thickness scaling. Alpha-particle-induced upsets (soft errors), once only the concern of dynamic memories, will affect static memories. Concern for latch-up will result in a wider spacing between devices than otherwise allowed by the scaled technology resulting in a loss in density.

An SOI-based technology with a thin silicon film is an ideal solution for all the aforementioned problems and is therefore ideal for submicron CMOS applications. With a thin silicon film, device isolation can be achieved by a complete-island-etch process without introducing a severe variation in the topography. By scaling the thickness of the surface silicon film with the gate length, the roll-off of the threshold voltage in SIMOX devices is very small. SIMOX/CMOS devices with gate length as low as 0.25 μm have been fabricated with excellent characteristics. A slope for subthreshold drain current approaching the theoretical value of 60 mV/dec can be obtained in MOSFET devices fabricated in a thin-film SOI structure [14]. This result occurs because the thin-film SOI structure reduces the depletion charge under the gate structure. As a consequence, a device with a smaller threshold voltage can be fabricated, making it possible to increase circuit speed without sacrificing the standby power performance.

The thin-film SOI structure also results in a drastic reduction in hot-electron effects in nMOS devices [15]. This is due to a decrease in the drain electric field.

Minimizing hot-electron effects yields a more reliable circuit and allows more aggressive scaling of the gate oxide to further enhance speed. The same properties that make SOI-based CMOS structures tolerant to transient radiation will yield devices that are highly resistant to alpha-particle-induced soft errors. Therefore, the potential exists for soft-error resistance without design compromise in speed and density.

1.3.4 Novel-Device Applications

The flexibility of SOI technology extends beyond the adaption of existing devices to SOI substrate. Novel device possibilities have recently been demonstrated, which can hardly or not be made in bulk silicon. These novel device structures are briefly summarized as follows:

- Voltage-controlled bipolar-MOS devices (VCBM) [16]. VCBM is realized by connecting the gate of the MOS device to the body node of the MOS device. Consequently, the body node of the MOS device becomes the base of the bipolar device. Similarly, the source and drain of the MOS device become the emitter and the collector of the bipolar device, respectively. The advantage of VCBM is taken of both MOSFET and lateral bipolar effect to obtain maximum current drive capability. The use of a VCBM logic would permit an increase in circuit speed by reducing the supply voltage and logic swing without decreasing current-drive capability. The absence of a floating substrate in the VCBM device may also improve device stability under harsh environment conditions.

- Dual-gate volume-inversion MOSFET (VI-MOSFET) [17]. When the silicon film of SOI structure is thin enough, inversion can be achieved across the whole film. Therefore, the current drive of VI-MOSFET is governed by minority carriers confined at the film rather than at an interface. Such a device presents tremendous advantages: (i) greatly increased number of minority carriers allowing higher current; (ii) reduced influence of surface-related scattering events; and (iii) enhanced effective mobility and transconductance. Moreover, for extremely

thin silicon film, quantum well MOSFET may be achieved.

- Single-transistor memory cell (STMC) [18]. The floating body effect and the dual gate configuration of SOI MOSFET provide a deep depletion condition to be created by appropriate front and back gate biasing. As the STMC sustains a memory function, it can be used to build memory devices. In contrast to a DRAM cell, which essentially consists of a transistor and a charge-holding capacitor, the basic STMC can be regarded as a charge-holding capacitor (the SOI body) with a transistor on top of it, integrated in only one device. Charge retention in the order of hours and longer, depending on temperature and operational conditions, is observed in recrystallized SOI technology.

- SOI waveguide [19]. Crystalline silicon, surrounded by lower-index claddings (such as SiO_2), is a low-loss waveguide for infrared light in the 1.3 to 10 μm wavelength range. SOI is a natural candidate for such a waveguide. By integrating silicon guided-wave components and silicon electronics on the SOI substrate, optical interconnections are possible. (For the 1.3 μm wavelength, silicon light emitting diodes and Schottky-barrier photodiodes have been developed [20].)

Several novel device structures have also been reported, such as p-i-n photodetector [21], lubistor, and induced collector bipolar transistor [22]. Three-dimensional ICs for CMOS-SRAM and parallel image processing have also been designed and fabricated [23]. Due to its flexibility, SOI is a material of choice for exploring new device physics and the properties of silicon.

1.4 Synopsis of Chapters

This dissertation mainly deals with the analytical and numerical modeling of SOI devices for material and device characterization. It consists of two parts. In the first part, several electrical characterization techniques using test structures such as diode,

capacitor, and MOSFET for evaluating the film and the interface properties of the SOI materials and devices are developed. In the second part, the design considerations for improved VLSI circuit manufacturability in SOI MOSFETs are discussed.

The work that follows is presented in five chapters. Chapter 2 describes the use of the SOI diode as a test vehicle for evaluating the quality of SOI substrates. In this chapter, a differential technique that uses reverse biased current-voltage and capacitance-voltage measurements on a p-n junction or a Schottky-barrier diode is developed for determining the generation lifetime profile in thin semiconductor films. It is shown that the bias independent leakage current can be eliminated by this differential technique. Furthermore, any error caused by field-enhanced current can be estimated. The properties of film/buried oxide interface also can be determined by using the gated diode measurements. These measurements are made by changing the back gate (substrate) bias while keeping diode reverse bias fixed.

Chapters 3 and 4 summarize the use of silicon-insulator-silicon (SIS) capacitor as a test structure for evaluating both buried oxide interfaces and film properties of the SOI substrates. In Chapter 3, a model is developed for electrical characterization of interface properties in a SIS capacitor using capacitance and conductance methods. By introducing a coupling factor, conventional metal-oxide-semiconductor (MOS) capacitor theory is modified and applied to analyze the properties of the film/buried oxide (F/O) and substrate/buried oxide (S/O) interfaces of a SIS capacitor. Theoretical expressions for extracting interface parameters are derived, which clearly show the effect of charge coupling between two semiconductors. The model enables us to extract doping concentration, buried oxide thickness, fixed oxide charge, and interface state density from the static and dynamic capacitance and conductance measurements on a simple SIS capacitor formed on the SIMOX substrate. In Chapter 4 transient capacitance techniques are modified for the characterization of the SIS capacitor. It consists of conventional Zerbst, temperature-scan DLTS, and bias-scan DLTS tech-

niques for both bulk and interface state characterization. Methods of distinguishing among different sources of transient signals such as bulk traps, interface states, and minority carrier generation are discussed. Using these techniques we have determined generation lifetime, localized state and interface state densities of SIMOX based SIS capacitors at both the F/O and the S/O interfaces.

In Chapter 5 simple techniques for evaluating the interface state density in small geometry MOSFETs operating in the linear region are discussed. Interface state densities determined by high- and/or low-frequency transconductance measurements for both bulk and SOI MOSFETs are presented. Chapter 6 compares the production yield of the bulk and the SOI VLSI circuits. The production yield of VLSI circuits is investigated by examining the statistical variation of the threshold voltage induced by random distributed device parameters. The analysis reveals that thin-film SOI MOSFET is less sensitive to inherent fluctuations in device parameters. Design considerations in minimizing the statistical threshold voltage variation in SOI MOSFETs are discussed. By properly choosing the gate material, film thickness, and channel doping density, enhancement of production yield can be expected for high performance SOI VLSI circuits. Chapter 7 gives the conclusions reached in this dissertation.

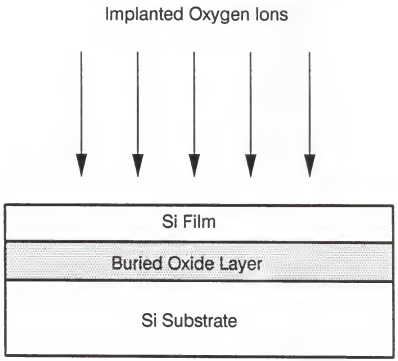

Figure 1.1 Implanted oxygen ion process for the fabrication of a SIMOX wafer.

CHAPTER 2
DETERMINATION OF GENERATION LIFETIME PROFILE IN THIN SEMICONDUCTOR FILMS

2.1 Introduction

In this chapter we present a simple differential technique for determining the generation lifetime profile in thin semiconductor films. The method described here involves a combination of current-voltage (I-V) and capacitance-voltage (C-V) measurements on a reverse-biased diode. The generation lifetime τ_g as a function of the bias voltage is extracted from the I-V characteristic and the position is related to the bias voltage by the C-V characteristic. Furthermore, the gated-diode technique is applied to the SOI diode for characterizing the film/buried oxide interface. The test structures suitable for the proposed technique include thin film junction diode, p-i-n diode, back-surface-field solar cell, and bipolar transistor.

2.2 Currents in Reverse-Biased p-n Junction

The current flowing through a reverse-biased p-n junction may consist of several components. The principal of which are:

- Diffusion current (I_{diff}): due to carrier generation in the neutral regions.
- Generation current (I_g): due to carrier generation inside the depletion layer.
- Multiplication current (I_m): due to production of electron-hole pairs by collision of carriers injected into the depletion layer with the lattice atoms.
- Field emitted current (I_{fe}): due to band-to-band electron tunnelling.

- 'Leakage current': due to several phenomena occurring at the surface, such as surface generation-recombination effects, surface channels, and effects related to the presence of the oxide.

Usually the reverse current components are not of the same importance. The field emitted current is negligible whenever the doping concentrations are not extremely high, and in wide band gap semiconductors diffusion currents are much smaller than generation currents up to temperatures some ten degrees in excess of room temperature. Moreover, at reverse voltages not greater than 2/3 the breakdown voltage, the multiplication current too may be neglected. Therefore, reverse current measurements performed on a silicon p-n junction usually yield the sum of the generation and the 'leakage' currents. On the other hand, when the 'leakage' current is negligible, as happens for devices with large area-to-circumference ratios, reverse current and junction capacitance measurements could give very useful information on generation-recombination centers.

It is well known that the generation current in a reverse-biased diode can be evaluated using the Sah-Noyce-Shockley model [24]. Therefore, the generation current can be expressed by

$$I_g = qUW \tag{2.1}$$

where q is the electronic charge, U is the carrier generation rate, and W is the depletion layer width. The generation current varies with the applied voltage in the same way as the depletion layer width W. Since the junction capacitance C is inversely proportional to the depletion layer width W, the product of bulk generation current and junction capacitance should be independent of the applied reverse bias voltage. However, this behavior has not been reported in the literature. The discrepancy has been explained by the domination of the surface leakage [25] and by a field dependent generation lifetime [26]. Calzolar and Graffi [27] have attributed an important cause of the discrepancy to the considerable difference existing between the depletion layer

width W and the generation layer width W_i. It was shown that the generation rate drops rapidly to negligible values outside W_i, but that W_i is not the same as W.

2.3 Theory

2.3.1 Evaluation of Generation Layer Width

Although the quasi-Fermi levels are not constant through the whole depletion layer, as happen for forward or weak reverse bias, they are, however, constant beyond the point of intersection with the potential curve where the corresponding carrier concentration takes the value n_i (intrinsic carrier concentration). Calzolar and Graffi [27] have shown that, by one-dimensional numerical analysis, the carrier generation rate U is constant over an interval W_i considerably smaller than W, dropping rapidly outside it, and that a good evaluation of W_i is represented by the distance between the intersections of the potential with the quasi-Fermi levels. In short we may say that the generation rate, being strongly dependent on the carrier concentrations, keeps practically constant at its maximum value when

$$p, n \ll n_i \tag{2.2}$$

and drops to negligible values as soon as (2.2) is not fulfilled, so that the width W_i is reasonably well defined by intersections of the potential with the quasi-Fermi levels. On the other hand, the depletion layer width W, to be employed in charge and capacitance calculations, must be defined with reference to

$$p, n \ll |N_d - N_a| \tag{2.3}$$

and, as $|N_d - N_a|$ may be greater than n_i by several orders of magnitude, W_i is usually considerably smaller than W.

In a p-n junction located at $x = 0$, let N_a be the acceptor concentration for $x < 0$ and N_d the donor concentration for $x > 0$. If the depleted region extends from $-x_1$

to x_2 (see Fig. 2.1), the potential can be expressed by

$$\psi(x) = \frac{qN_a}{2\epsilon_s}(x + x_1)^2 \qquad -x_1 \leq x \leq 0 \tag{2.4}$$

$$\psi(x) = \psi_o + V_r - \frac{qN_d}{2\epsilon_s}(x_2 - x)^2 \qquad 0 \leq x \leq x_2 \tag{2.5}$$

having assumed $\psi(-x_1) = 0$, $\psi(x_2) = \psi_o + V_r$, and the electric field vanishing at the depletion layer edges. ψ_o and V_r represent the build-in potential and the applied reverse voltage, respectively.

Continuity of the potential and of the electric field in the origin permits evaluation of x_1, x_2 and $W = x_1 + x_2$. These relationships are given as

$$x_1 = \frac{N_d}{N_a + N_d}W \tag{2.6}$$

$$x_2 = \frac{N_a}{N_a + N_d}W \tag{2.7}$$

$$W = \left[\frac{2\epsilon_s}{q}\frac{N_a + N_d}{N_a N_d}(\psi_o + V_r)\right]^{1/2} \tag{2.8}$$

In order to calculate $W_i = x_{2i} - x_{1i}$, one has to solve the equations

$$\psi(x_{1i}) = \phi_p, \qquad \psi(x_{2i}) = \phi_n \tag{2.9}$$

where ϕ_n and ϕ_p are constants given by

$$\phi_p = \frac{kT}{q}\ln\frac{N_a}{n_i} \tag{2.10}$$

$$\phi_n = \psi_o + V_r - \frac{kT}{q}\ln\frac{N_d}{n_i} \tag{2.11}$$

Substituting (2.5) in (2.9) brings out the following pair of relations [27]

$$x_2 - x_{1i} = \left[\frac{2\epsilon_s}{qN_d}\left(V_r + \frac{kT}{q}\ln\frac{N_d}{n_i}\right)\right]^{1/2} \tag{2.12}$$

$$x_2 - x_{2i} = \left[\frac{2\epsilon_s}{qN_d}\frac{kT}{q}\ln\frac{N_d}{n_i}\right]^{1/2} \tag{2.13}$$

where a p^+-n abrupt junction is assumed. From (2.12) and (2.13), we can express the generation layer width as [27]

$$W_i = \left(\frac{2\epsilon_s kT}{q^2 N_d}\right)^{1/2}\left[\left(\ln\frac{N_d}{n_i} + \frac{qV_r}{kT}\right)^{1/2} - \left(\ln\frac{N_d}{n_i}\right)^{1/2}\right] \tag{2.14}$$

Equations (2.8) and (2.14) show that both W and W_i depend on the square root of the applied voltage for large reverse bias, and the difference between the two quantities becomes less significant at high reverse bias. Figure 2.2 shows the ratio W_i/W as a function of reverse voltage for several donor concentrations in a p^+-n abrupt junction. It is noted that W differs from W_i in a wide range of reverse-bias voltages. This figure gives evidence to the fact that the current-capacitance product is far from being constant up to voltages in excess of 100 V.

2.3.2 Generation Lifetime Profile Technique

A schematic representation of the preferred types of device structures, but not limited to these structures, for which the generation lifetime profile technique can be used is shown in Fig. 2.3. The structure shown in Fig. 2.3(a) consists of a thin n-type epitaxial layer grown on a conducting substrate, such as p- or n^+- type semiconductor. This structure is relevant, for example, to bipolar transistors and back-surface-field solar cells. The other device structure shown in Fig. 2.3(b) consists of an n-type epitaxial layer grown on top of an insulating substrate, such as the semi-insulating GaAs or silicon-on-insulator substrate. A p^+-n junction or a Schottky diode is formed on top of the epitaxial layer for I-V and C-V measurements. These structures prohibit further extension of the depletion region when the epilayer is fully depleted and hence provide an easy way to identify the field dependent current components.

The current flowing through a reverse-biased diode may consist of several components, which include the diffusion current I_{diff}, the bulk generation current I_g^b, the surface generation current I_g^s, the multiplication current I_m and the field-emitted current I_{fe}. For a p^+-n diode, with an applied reverse bias V_r, the total reverse current can be simply expressed by

$$I_r(V_r) = A_s q n_i s_f + A_b q \int_0^{W_i(V_r)} \frac{n_i}{\tau_g(x)} dx \qquad (2.15)$$

where s_f is the top surface generation velocity, A_b is the area of the bulk space charge region, and A_s is the surface area of the diode. The diffusion current is negligible due

to small intrinsic carrier concentration of silicon [28]. The multiplication current is significant only when V_r is large. The field-emitted current is negligible whenever the doping concentrations are not extremely high.

We can express (2.15) in a differential form by using $dW/dV_r = (\epsilon_s A_b/C^2)dC/dV_r$. In terms of the measurable quantities, the generation lifetime can then be expressed by

$$\tau_g(W_i) = \frac{\epsilon_s q n_i A_b^2}{C^2} \frac{dW_i}{dW} \frac{dC/dV_r}{dI_r/dV_r} \tag{2.16}$$

where

$$\frac{dW_i}{dW} = \left[\frac{V_r + (kT/q)\ln(N_a N_d/n_i^2)}{V_r + (kT/q)\ln(N_d/n_i)} \right]^{1/2} \tag{2.17}$$

is the correction factor, which takes into account the difference in the variation of W_i and W. It is noted that even though W_i may differ from W significantly, $dW_i/dW \simeq 1$ for a wide range of bias voltages and doping concentrations N_d.

2.4 Results and Discussion

The starting silicon substrate has a resistivity of 3-5 Ω-cm. The buried-oxide layer was produced by implanting O^+ ions using Eaton NV-200 oxygen implanter. The wafer temperature was maintained at 500°C by beam heating during oxygen implantation. The implant energy was 150 keV, and the oxygen doses of 1.8 and 2.0 $\times 10^{18}$ cm^{-2} were used. High-temperature annealing (1250 or 1285°C, 2 hours) was applied to the wafer following oxygen implantation. N-type silicon epitaxial layers of thickness ranging from 1.3 to 1.7 μm were grown on these SIMOX wafers. The p^+-n diodes were formed in the SIMOX substrates with a junction depth of 0.4 $\pm$ 0.1 μm and junction area of 450 $\times$ 450 μm^2. The I-V and C-V measurements were carried out at room temperature using HP 4140 pA meter and HP 4280A C meter, with the substrate grounded.

We have examined more than sixty devices receiving different implantation and post implantation annealing treatments. Figure 2.4 shows the C-V characteristics

of a typical SOI diode with back gate (substrate) bias V_{Gb} as a parameter. The top silicon film is fully depleted at $V_r \sim 1V$ for $V_{Gb} = 0$, as is estimated from the hump of the C-V curve. The inset shows the corresponding free carrier concentration profiles determined by the differential capacitance technique. Carrier concentration is generally uniform across the epitaxial layer except near the buried oxide layer where the fixed oxide charge tends to attract free carriers toward the interface. The effect of series resistance in C-V measurement was taken into account by considering both capacitive and resistive components of the diode [29]. Also, a positive back-gate bias was applied to accumulate the film/buried oxide (F/O) interface, which in turn significantly reduced the series resistance and provided a very accurate doping concentration profile beyond a distance of 0.2 μm from the F/O interface. The doping concentration in this region is shown by the differential capacitance technique to be uniform.

Typical I-V characteristics are shown in Fig. 2.5. Sample A is a bulk diode and samples B, C, and D are SIMOX diodes. It is noted that sample D is the most recently implanted sample that is expected to have a lower contamination level due to modification in the implanter [30]. The I-V curves of SIMOX diodes are normalized to the reach-through voltage V_{rt} (determined by the corner of reverse I-V characteristics) and the corresponding current I_{rt}. These values along with the different implantation and post implantation annealing parameters are summarized in Table 2.1. For $V_r > V_{rt}$, I_r is nearly constant due to reach-through of silicon film. A slight increase of I_r in this region is due to the contribution of field dependent currents.

The generation lifetime profile is determined by using (2.16) with the assumption of uniform doping concentration. The result is shown in Fig. 2.6. Sample A (bulk diode) has uniform τ_g for a distance of about 2 μm, and the value is close to that reported by Schroder [31]. Samples C and D show a significant increase of generation

current as V_r approaches V_{rt}, indicating a significant reduction of τ_g as the buried oxide layer is approached. Sample B has I-V characteristics similar to that of bulk diode for $V_r < V_{rt}$, and has a relative uniform τ_g compared to that of samples C and D. It is noted that a dramatic reduction of τ_g within a Debye length ($\sim 0.1\mu m$) from the F/O interface in sample D is predominantly caused by the generation current from the F/O interface states. This phenomenon is not seen in sample B and C, since bulk generation current dominates over the F/O interface generation current. This result is confirmed by the gated diode measurements shown in Fig. 2.7. These measurements are made by changing the back gate bias V_{Gb} while keeping V_r fixed. When the F/O interface is accumulated or inverted, only those centers which are within the film contribute to the generation current. However, while the F/O interface is depleted, interface generation provides yet another contribution to the total generation current. This contribution will result in a peak in I_r versus V_{Gb} characteristics. It is noted that this peak can only be observed in sample D rather than samples B and C.

An estimation of the F/O interface generation velocity s_b can be made on the basis of the Sah-Noyce-Shockley theory of the recombination-generation process [24]. From the generation current at the F/O interface of Fig. 2.7, the interface generation velocity of the depleted interface was found to be of $s_b = 12.8$ cm/s. If an effective capture cross-section $\sigma = 10^{-16}$ cm^2 is assumed, the above value is equivalent to a density of single level interface states $D_{it} \simeq 10^{10}$ cm^{-2}. Alternatively, it is also equivalent to a uniform distribution of interface states with density $D_{it} \simeq 10^{11}$ cm^{-2}eV^{-1} [32].

By measuring the temperature dependence of the reverse-biased current generated from the film and the F/O interface, the energy level of these generation-recombination centers can be determined. As is shown in Fig. 2.8, the temperature dependence of generation currents gives apparent activation energies of $E_a = 0.41$ and 0.48 eV for the film and the F/O interface, respectively. The origin of the traps

in SIMOX film may be related to the metal impurities that are incorporated during the oxygen implantation. The metal impurities segregate to the F/O interface where they interact with the structure defects near the interface. This gettering process tends to change their electrical activity and defect configuration, leading to different temperature dependency of the generation current. Another possible source of interface generation current is related to the oxygen precipitates, dislocations, and silicon dangling bonds.

In Table 2.1, the generation lifetimes calculated by conventional Zerbst analysis of capacitance transients on the buried oxide capacitor [33] are included for comparison. The Zerbst lifetimes and the lifetimes determined by present technique are in reasonable agreement for the corresponding samples measured. The discrepancy of τ_g determined by Zerbst method and by the present technique in sample C is believed to be caused by film nonuniformity, while the discrepancy in sample D is attributed to the dominance of the F/O interface generation over the bulk generation. It is worth noting that in Zerbst method, a uniform generation lifetime is required to obtain an accurate value. Also, the short generation lifetime of sample C makes it very difficult to find a linear region to extract generation lifetime from the Zerbst plot. It is also noted that in sample B, which has a uniform generation lifetime, the agreement between these two techniques is significantly improved.

For $V_r > V_{rt}$, because the depletion layer width is essentially limited by the buried oxide layer, any increase in I_r can be attributed to field dependent currents. Therefore, an estimation of error can be obtained from this part of I-V characteristics. The increase of I_r at $V_{rt} < V_r < 2V_{rt}$ is less than 11 % of the total current which suggests an error of about the same magnitude. It is noted that the generation lifetime profile differs by order of magnitude for samples C and D. The error caused by field dependent currents is essentially negligible in our analysis.

2.5 Conclusion

In conclusion we have proposed and demonstrated a current-capacitance technique for analyzing generation lifetime profile in thin semiconductor films. The method requires only I-V and C-V measurements on a diode; it also provides a simple procedure for identifying any error caused by the field dependent currents. The buried interface generation velocity can also be determined by the gated diode technique. The spatial resolution of current-capacitance technique is identical to that of C-V profiling technique, which is about that of Debye length. We showed that current-capacitance technique is more plausible and accurate than the conventional Zerbst method for generation lifetime measurement. The method is simple and can be applied to either conducting or nonconducting substrates for rapid assessment of wafer quality prior to fully processing of the complex devices and circuits.

Table 2.1 Summary of processing and device parameters and Zerbst lifetimes for the bulk and SOI diodes.

Sample	Annealing	Dose (cm^{-2})	N_d (cm^{-3})	V_{rt} (V)	I_{rt} (A)	Zerbst τ_g^* (μs)
A (Bulk)			2.0×10^{15}	3.4	2.8×10^{-13}	
B (SIMOX)	1250°C, 2 hrs	1.8×10^{18}	1.6×10^{15}	3.4	2.3×10^{-9}	0.12
C (SIMOX)	1250°C, 2 hrs	2.0×10^{18}	3.0×10^{15}	1.8	7.3×10^{-7}	0.02
D (SIMOX)	1285°C, 2 hrs	1.8×10^{18}	1.6×10^{15}	1.0	5.8×10^{-11}	4.4

$*$ Note: The Zerbst lifetimes are calculated at 0.4 ± 0.1 μm from the film/buried-oxide interface.

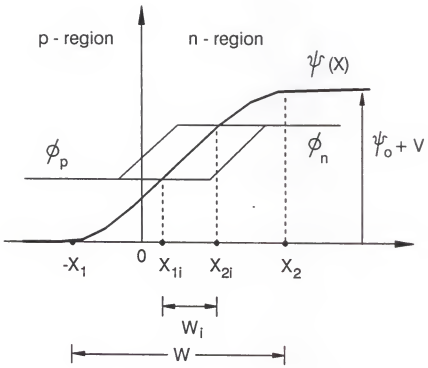

Figure 2.1 Schematic representation of potential and quasi-Fermi levels in a one-sided abrupt junction.

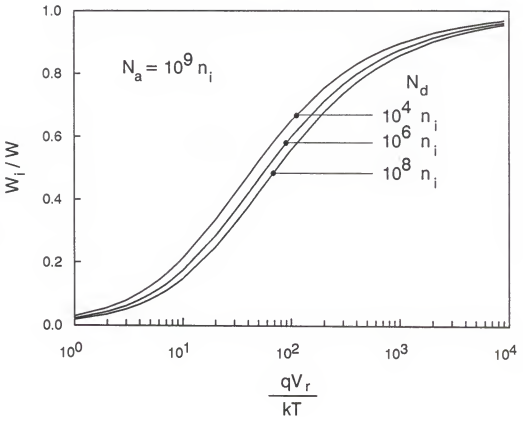

Figure 2.2 The ratio of generation layer width W_i to depletion layer width W as a function of reverse voltage for several donor concentrations in a p^+-n abrupt junction [27].

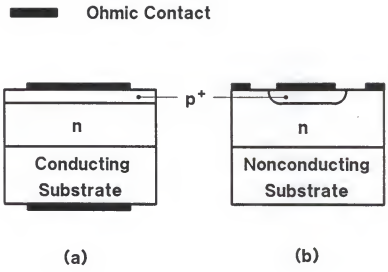

Figure 2.3 Schematic representation of the two structures with a thin epitaxial n-type layer grown on top of (a) a conducting substrate, such as n^+ or p type semiconductor, and (b) an insulating substrate, such as semi-insulating GaAs or silicon-on-insulator substrate.

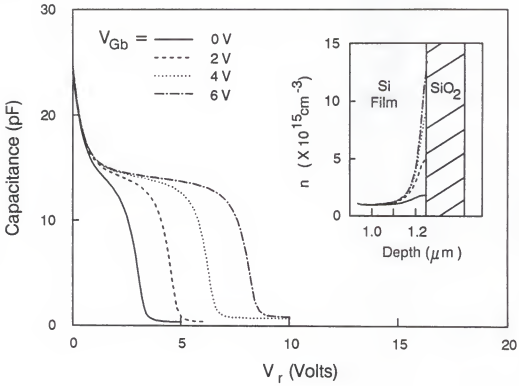

Figure 2.4 Capacitance-voltage characteristics of p^+n SOI diode with back gate bias V_{Gb} as a parameter. The inset shows the corresponding free carrier concentration profiles.

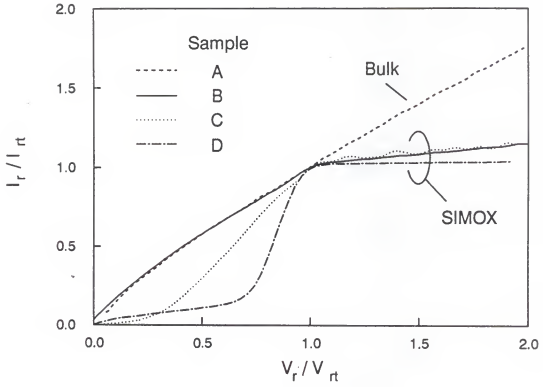

Figure 2.5 Normalized reverse bias current-voltage characteristics. The voltage is normalized to the reach-through voltage V_{rt}, and the current is normalized to the corresponding reach-through current I_{rt}.

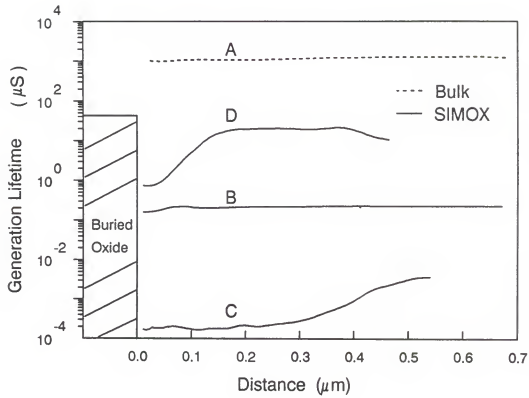

Figure 2.6 Generation lifetime versus distance from the film/buried oxide interface. Sample A is arbitrarily positioned on the distance axis for comparison. Processing and device parameters for these samples are summarized in Table 2.1.

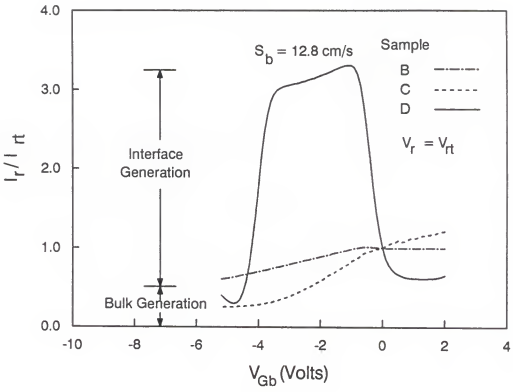

Figure 2.7 Normalized reverse current as a function of back-gate bias V_{Gb}.

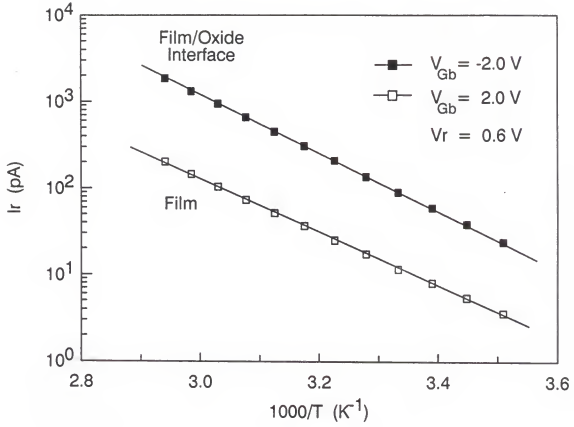

Figure 2.8 Temperature dependence of the reverse current generated from the film and film/buried oxide interface.

CHAPTER 3
A MODEL FOR ANALYZING THE INTERFACE PROPERTIES OF A SEMICONDUCTOR-INSULATOR-SEMICONDUCTOR STRUCTURE: CAPACITANCE AND CONDUCTANCE TECHNIQUES

3.1 Introduction

Recent progress in the formation of SOI substrates using separation by implantation of oxygen (SIMOX) technology has led to the fabrication of devices on ultra-thin silicon film [34,35]. As the film thickness is greatly reduced, the interface properties of the SOI structure become more and more influential to the device performance [36]. Most of the characterization works reported for SIMOX and other SOI technologies have been focused on the microstructures of buried oxide [37] and the transport properties and bulk traps in the top silicon film [38,39]. Only few researchers have investigated the fixed oxide charge and interface traps at either oxide interfaces by either capacitance [40,41], transconductance [42,43], or charge-pumping techniques [44].

In this chapter we present a model for electrical characterization of film/buried-oxide/substrate interfaces of the SIMOX based SOI substrates. The approach is based on the modification of the conventional MOS capacitor theory to the two Si/SiO_2 interfaces of a semiconductor-insulator-semiconductor (SIS) capacitor. By introducing a coupling factor, which relates the surface potentials of both interfaces, the small signal equivalent circuit of a SIS capacitor can be reduced to a MOS-like equivalent circuit. Based on this model, the expressions for relating the surface potential to the gate bias and for extracting the interface trap density and doping concentration from the capacitance and conductance measurements are derived. Device parameters

such as doping concentration, oxide thickness, fixed oxide charge, and interface trap density can be determined from these measurements. Results of the capacitance and conductance measurements on the SIMOX SIS capacitors are discussed. Our analysis shows that neglecting charge coupling between the top and the bottom interfaces of a SIS capacitor can result in underestimation of the interface trap densities at both interfaces.

3.2 Small Signal Equivalent Circuits

In this section, we present a small signal model applicable for an n-Si/SiO_2/n-Si (n-i-n) SIS capacitor structure. In general, this model can be applied to other semiconductor-insulator systems or an n-i-p structure. For simplicity, we shall refer to the top silicon film (F) as semiconductor 1 (S1) and the substrate (S) as semiconductor 2 (S2). Several assumptions are made in the following analysis. These include: (i) doping densities in both S1 and S2 are uniform, (ii) the gate bias is applied to S1 with reference to S2 as shown in Fig. 3.1, (iii) the difference in the metal and semiconductor work functions of the ohmic contact is identical at S1 and S2, (iv) surface potential as a function of d.c. gate bias is independent of the frequency of small signal gate bias, (v) there are no mobile ions in the buried oxide layer, and (vi) the buried oxide layer is a perfect insulator and the effects due to leakage current, space charge and polarized molecules in the buried oxide are negligible.

Figure 3.1 shows the energy band diagram for a SIS capacitor structure used in this study. If a gate bias V_G is applied to the film and the substrate is grounded, then a set of equations can be derived from the global equilibrium and Gauss' law [40,45]

$$V_G = \psi_{s2} - \psi_{s1} + V_{ox} + W_{12} \tag{3.1}$$

$$Q_T = Q_{s1} + Q_{it1} + Q_{f1} = -Q_{s2} - Q_{it2} - Q_{f2} \tag{3.2}$$

$$V_{ox} = Q_T / C_{ox} \tag{3.3}$$

$$W_{12} = \frac{kT}{q}\ln(\frac{N_{d2}}{N_{d1}}) \tag{3.4}$$

where ψ_s is the surface potential, Q_T is the total charge held by the buried oxide capacitor, V_{ox} is the potential drop across the buried oxide, W_{12} is the Fermi potential difference between S1 and S2; N_d, Q_s, Q_{it}, and Q_f denote the doping density, surface charge, interface trapped charge, and fixed oxide charge, respectively. In (3.1) $\sim$ (3.4), subscripts 1 and 2 denote the interfaces of S1 and S2, respectively. The total capacitance of a SIS capacitor C_T can be expressed by [40,45]

$$\frac{1}{C_T} = \frac{1}{C_{s1} + C_{it1}} + \frac{1}{C_{ox}} + \frac{1}{C_{s2} + C_{it2}} \tag{3.5}$$

where $C_s(= -dQ_s/d\psi_s)$ is the surface capacitance, $C_{it}(= -dQ_{it}/d\psi_s)$ is the static capacitance of the interface trap, and C_{ox} is the buried oxide capacitance. In the following analysis, we consider the case of a negative gate bias which tends to deplete S2. Similar analysis may be applied for a positive bias which tends to deplete S1.

As the gate bias is varied, the surface potential at both interfaces will also change. The coupling of the surface potentials not only depends on silicon properties, but also on interface properties (i.e., interface trap and fixed oxide charge). Our approach is to introduce a coupling factor defined by

$$K_2(\psi_{s2}) \equiv \frac{d\psi_{s1}}{d\psi_{s2}} \tag{3.6}$$

which describes the charge coupling of the film/buried-oxide/substrate interfaces. Coupling factor can also be expressed in terms of C_s and C_{it} by differentiating (3.2) with respect to ψ_s, which yields

$$K_2(\psi_{s2}) = -\frac{C_{s2} + C_{it2}}{C_{s1} + C_{it1}} \tag{3.7}$$

In analogy to the MOS theory [46], $d\psi_{s2}/dV_G$ can be expressed in terms of the surface capacitance and interface trap capacitance by differentiating the charge conservation relation with respect to surface potential:

$$\frac{d\psi_{s2}}{dV_G} = -\frac{C_{ox}}{C_{s2} + C_{it2} + C_{ox}(1 - K_2)} \tag{3.8}$$

Using (3.8) or substituting (3.7) into (3.5), the total capacitance of a SIS capacitor can be expressed by

$$\frac{1}{C_T} = \frac{1}{C_{ox}} + \frac{1 - K_2}{C_{s2} + C_{it2}} \tag{3.9}$$

Therefore, the equivalent circuit of a SIS capacitor can be reduced to a MOS-like equivalent circuit using (3.9), as shown in Fig. 3.2. If $K_2 = 0$, then the equivalent circuit shown in Fig. 3.2 will reduce to the conventional MOS equivalent circuit.

3.3 Extraction of Interface State Parameters

In this section we discuss how the interface trap density as a function of gate bias or surface potential can be determined from the measured admittance of a SIS capacitor. There are four different methods for extracting interface trap parameters [46]: the high-frequency capacitance, low-frequency capacitance, combined high-low frequency capacitance, and conductance methods. These methods are discussed separately as follows:

3.3.1 Capacitance Method

In analogy to high-frequency MOS capacitance method developed by Terman [47], the interface trap capacitance can be determined from (3.1) $\sim$ (3.4) as

$$C_{it2}(\psi_{s2}) = C_{ox}\left[(\frac{d\psi_{s2}}{dV_G})^{-1} + K_2 - 1\right] - C_{s2}(\psi_{s2}) \tag{3.10}$$

It is noted that if $K_2(\psi_{s2})$ and ψ_{s2} versus V_G are determined, then C_{it2} can be determined.

At frequencies low enough that the interface traps can follow the a.c. bias, the C-V characteristics are represented by the equivalent circuit shown in Fig. 3.2. Using this equivalent circuit, C_{it2} can be determined from the measured low-frequency capacitance data [48,49], provided that $C_{s2}(V_G)$ and $K_2(V_G)$ are known. Solving (3.9) for C_{it2} yields

$$C_{it2}(V_G) = (1 - K_2)\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - C_{s2}(V_G) \tag{3.11}$$

where C_{LF} is the low frequency capacitance measured at a gate bias V_G. Value of $C_{s2}(V_G)$ can be determined by theoretical calculation. This can be carried out by first calculating C_{s2} as a function of ψ_{s2} using conventional MOS theory and then relating $C_{s2}(\psi_{s2})$ to $C_{s2}(V_G)$, providing that ψ_{s2} versus V_G is known.

We can also apply the combined high-low frequency capacitance method of the MOS theory [48,49] to a SIS capacitor. In this approach, the high-frequency capacitance is obtained from (3.9) by setting $C_{it}(\omega) = 0$, and the result yields

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1 - K_2}{C_{s2}} \tag{3.12}$$

Now solving (3.12) for C_{s2} and then substituting it into (3.11), we obtain

$$C_{it2}(V_G) = (1 - K_2)\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}\right] \tag{3.13}$$

Using (3.13), C_{it2} is obtained directly from the C-V measurements. This approach eliminates the uncertainties introduced by using the calculated C_{s2}, which requires the knowledge of correct band bending.

3.3.2 Conductance Method

The conductance method [46,50] can be used to determine the interface trap density in a SIS capacitor. The following analysis was made for the SIS capacitor operating in the depletion region. Let Q_T be the total charge density held by the buried oxide capacitor at a given bias. The ac current density, $i_T(t)$, obtained by differentiating (3.2) with respect to time, is given by

$$\begin{aligned} i_T(t) &= \frac{dQ_T}{dt} \\ &= (j\omega C_{D2} + Y_{it2})\partial\psi_{s2} \end{aligned} \tag{3.14}$$

where C_{D2} is the depletion layer capacitance, Y_{it2} is the admittance of a series RC network associated with interface traps, which is a function of surface potential. By differentiating (3.1) with respect to time, we obtain

$$\partial V_G = \partial\psi_{s2} - \partial\psi_{s1} + \frac{i_T(t)}{j\omega C_{ox}} \tag{3.15}$$

Substituting $\partial\psi_{s2}$ from (3.14) into (3.15) yields

$$\partial V_G = \left[Z_{s2}(1 - K_2) + \frac{1}{j\omega C_{ox}} \right] i_T(t) \tag{3.16}$$

where K_2 is given by (3.7) and

$$Z_{s2} = (j\omega C_{D2} + Y_{it2})^{-1} \tag{3.17}$$

The term in the bracket of (3.16) is the impedance of the equivalent circuit in which C_{ox} is in series with $Z_{s2}(1 - K_2)$. The equivalent circuit for the SIS capacitor derived from (3.14) and (3.16) is shown in Fig. 3.3, where C_{it2} and G_{it2} are the capacitance and conductance associated with the interface traps at S2, respectively.

The interface state time constant τ_{it} defined by C_{it2}/G_{it2} can be used to predict the frequency behavior of the interface traps. The parallel branch of the equivalent circuit shown in Fig. 3.3 can be converted into a frequency-dependent capacitance C_p in parallel with a frequency-dependent conductance G_p, which are given by

$$C_p = (1 - K_2)^{-1} \left(C_{D2} + \frac{C_{it2}}{1 + \omega^2 \tau_{it}^2} \right) \tag{3.18}$$

and

$$\frac{G_p}{\omega} = (1 - K_2)^{-1} \left(\frac{C_{it2}\omega\tau_{it}}{1 + \omega^2 \tau_{it}^2} \right) \tag{3.19}$$

If we take interface trap continuum into account and assume that $(1 - K_2)$ is a slowly varying function of surface potential in a range of kT/q around the Fermi level, we obtain

$$C_p = (1 - K_2)^{-1} \left[C_{D2} + \frac{C_{it2}}{\omega\tau_{it}} \tan^{-1}(\omega\tau_{it}) \right] \tag{3.20}$$

and

$$\frac{G_p}{\omega} = (1 - K_2)^{-1} \left[\frac{C_{it2}}{2\omega\tau_{it}} \ln(1 + \omega^2 \tau_{it}^2) \right] \tag{3.21}$$

A comparison of the expressions for the capacitance and conductance methods in the MOS and SIS capacitors reveals that (3.10), (3.11), (3.13), and (3.21) differ from the MOS capacitor theory by a factor of $(1 - K_2)$. Thus, the conventional MOS

characterization methods can be extended to a SIS capacitor to obtain the interface trap density by simply multiplying the measured interface trap density by $(1 - K_2)$ to account for the charge coupling between the two interfaces of a SIS capacitor.

3.4 Coupling of Surface Potentials

To understand the capacitance and conductance methods described above, it is important to examine the physical aspects of coupling factor, since it contains all the information between the film, buried oxide layer, and the substrate of a SIS capacitor. For a given set of interface parameters (the fixed oxide charge and interface trap densities), ψ_{s1} and ψ_{s2} can be determined from (3.1) $\sim$ (3.4) for each gate bias. Therefore, C_{s1}, C_{s2}, C_{it1}, and C_{it2} as a function of surface potential can be calculated. From these results, coupling factor is determined by using (3.7).

Figures 3.4 and 3.5 show plots of absolute value of coupling factor as a function of ψ_{s2} with doping density as a parameter. Note that Q_{it} and Q_f are assumed equal to zero. In Fig. 3.4, the absolute value of coupling factor K_2 is plotted as a function of ψ_{s2} with identical doping density in S1 and S2. The relationship between ψ_{s1} and ψ_{s2} is also shown in Fig. 3.6. In spite of the apparent complexity of the coupling factor, it can be readily explained by focusing our attention on the flat band, accumulation, depletion, and the strong inversion regions to illustrate the underlying concepts.

Starting with zero gate bias, both interfaces are at the flat band condition, and $K_2 = -1$. As the gate bias becomes more positive, S1 is driven from depletion into weak inversion, and S2 is still in accumulation (region II). As a result, C_{s1} decreases and C_{s2} increases progressively, leading to an increase of $|K_2|$. At the onset of strong inversion in S1 (region I), the maximum depletion width is reached. In this case, C_{s1} saturates under high frequency operation, leading to a rapid increase of $|K_2|$. In the case of low frequency operation, C_{s1} also increases exponentially. The low frequency surface capacitances in S1 (strong inversion) and S2 (strong accumulation),

and coupling factor can be expressed as [46]

$$C_{s1} = \frac{C_{FBS}}{\sqrt{2}} \frac{n_i}{N_{d1}} \exp\left(-\frac{q\psi_{s1}}{2kT}\right) \tag{3.22}$$

$$C_{s2} = \frac{C_{FBS}}{\sqrt{2}} \exp\left(\frac{q\psi_{s2}}{2kT}\right) \tag{3.23}$$

and

$$K_2 = -\frac{N_{d1}}{n_i} \exp\left[\frac{q(\psi_{s1} + \psi_{s2})}{2kT}\right] \tag{3.24}$$

where C_{FBS} is the flat band surface capacitance and n_i is the intrinsic carrier concentration. For $\psi_{s1} < 0, \psi_{s2} > 0$ and $|\psi_{s1}| > \psi_{s2}$, a decrease of $|K_2|$ is expected. As the gate bias becomes negative, S1 is in accumulation and S2 in depletion (region III). Similar to the positive gate bias, a decrease of $|K_2|$ is obtained. At the onset of strong inversion in S2 (region IV), $|K_2|$ decreases in the case of high frequency operation and increases under low frequency operation. The effect of different doping concentrations on K_2 is also illustrated in Fig. 3.5. The result shows that for a given surface potential under depletion or weak inversion, $|K_2|$ is large when the doping concentration N_{d2} is high.

It is important to examine the region in which $|K_2|$ is less than 0.1, since, in this region, direct application of the conventional MOS theory to a SIS capacitor for determining the interface trap density would result in less than 10% error. We consider the upper half of the band gap, since the capacitance and conductance methods are applicable in this region. Note that in weak to moderate inversion, $|K_2|$ is generally smaller than 0.1. Figure 3.7 shows the energy region (relative to mid-gap) in which $|K_2|$ is equal to 0.1 as a function of N_{d2} with N_{d1} as a parameter. It should be noted that if the doping densities in both S1 and S2 are low, then the MOS theory is only applicable in an energy region of about 0.1 eV from the midgap. However, this energy range will widen as N_{d1} is increased. This is due to the reduced surface potential variation in S1 as N_{d1} is increased.

The coupling factor given in (3.7) can be approximated by

$$K_2' = -\frac{C_{s2}}{C_{s1}} \tag{3.25}$$

The error introduced by (3.25) is defined by

$$\text{Error} = \left| \frac{(1 - K_2) - (1 - K_2')}{(1 - K_2)} \right| \tag{3.26}$$

Now, substituting (3.7) and (3.25) into (3.26) yields

$$\text{Error} = \left| \frac{C_{s1}C_{it2} - C_{s2}C_{it1}}{C_{s1}(C_{s1} + C_{s2} + C_{it1} + C_{it2})} \right| \tag{3.27}$$

For small gate bias, it is generally true that $\psi_{s1} \simeq \psi_{s2} \simeq 0$ and $C_{s1} \simeq C_{s2} \gg C_{it}$, and thus (3.27) reduces to

$$\text{Error} \approx \left| \frac{C_{it2} - C_{it1}}{2C_{s2}} \right| \ll 1 \tag{3.28}$$

For a negative gate bias, S1 is in accumulation; with $C_{s1} \gg C_{s2}$ and $C_{s1} \gg C_{it}$, (3.27) becomes

$$\text{Error} \approx \left| \frac{C_{it2}}{C_{s1}} \right| \ll 1 \tag{3.29}$$

For a positive gate bias, S2 is in accumulation; with $C_{s2} \gg C_{s1}$ and $C_{s2} \gg C_{it}$, (3.27) reduces to

$$\text{Error} \approx \left| \frac{C_{it1}}{C_{s1}} \right| \tag{3.30}$$

Under high frequency operation $C_{it1} = C_{it2} = 0$, K_2 is equal to K_2'. Thus, the analysis presented here provides an upper limit of error for different operation frequencies and for different values of C_{it}.

Capacitance and conductance measurements are made in region II and III of Fig. 3.4 to avoid the frequency-dependent C_{s1} and C_{s2}. Figure 3.8 shows a plot of error (in percent) defined by (3.26) as a function of surface potential for four different values of donor concentration. As is shown, the error of using K_2' in the depletion region is less than 10% for $N_d > 10^{16}$ cm^{-3}. For $N_d = 10^{15}$ cm^{-3}, the maximum error is less than 18%. The exact correction factor can be obtained by using an approximated coupling

factor as a first trial value to obtain the corresponding interface trap densities, D_{it1} and D_{it2}, from the experiments. A new coupling factor is then obtained from (3.7). Finally, by using the iteration procedure, the accurate coupling factor can be determined.

3.5 Determination of Surface Potential Versus Gate Bias

In a MOS capacitor, the band bending as a function of gate bias can be directly determined from the low- and high- frequency capacitance method [46]. In a SIS capacitor, since two interfaces are involved, low-frequency capacitance method can only be used to determine the surface potential difference ($\Delta\psi_s \equiv \psi_{s2} - \psi_{s1}$) as a function of gate bias. In analogy to a MOS capacitor [51], this is given by

$$\frac{d(\psi_{s2} - \psi_{s1})}{dV_G} = 1 - \frac{C_{LF}}{C_{ox}} \tag{3.31}$$

Integrating (3.31), we obtain

$$\Delta\psi_s(V_G) = \Delta\psi_s(V_{GO}) + \int_{V_{GO}}^{V_G} dV_G \left[1 - \frac{C_{LF}(V_G)}{C_{ox}}\right] \tag{3.32}$$

Note that V_{GO} is chosen to minimize the uncertainty in $\Delta\psi_s(V_{GO})$. For example, V_{GO} can be chosen in accumulation or in inversion, where band bending is only a weak function of gate bias.

Once $\Delta\psi_s$ is determined, by using the charge conservation relation given in (3.1) $\sim$ (3.4), the surface potential can be determined by solving

$$Q_{s2}(\psi_{s2}) = C_{ox}[\Delta\psi_s - V_G + W_{12}] - [Q_{f2} + Q_{it2}] \tag{3.33}$$

The parameters on the right hand side of (3.33) can be determined experimentally. For example, fixed oxide charge is determined by the voltage shift of the C-V curve, surface potential difference is determined by integrating the low frequency C-V curve, and interface trapped charge is determined by integrating the interface trap density obtained from the high-low frequency capacitance measurement. Therefore, for a given gate bias, both ψ_{s1} and ψ_{s2} can be determined.

The band bending can also be determined by using high-frequency capacitance method (Terman's method [47]). Using (3.1) $\sim$ (3.4), the theoretical high-frequency $C - \psi_{s1}$ and $C - \psi_{s2}$ curves (taking the fixed oxide charge into account) can be generated. The results are then compared with the measured high frequency *C-V* curves to obtain ψ_{s1} and ψ_{s2} versus gate bias. It is worth noting that, this procedure is true only for $Q_{s1} + Q_{f1} \gg Q_{it1}$. This condition can be easily satisfied, since fixed oxide charge density is generally higher than the integrated interface trap charge [40]. Furthermore Q_{s1} increases exponentially with surface potential in accumulation, a small deviation from the flat band can satisfy the above requirement.

3.6 Determination of the SIS Capacitor Parameters

Prior to extract the interface parameters, the buried oxide thickness, doping concentration, and the fixed oxide charge need to be determined experimentally. Buried oxide thickness of a SIS capacitor can be determined by three different methods. First, if the doping concentration in either S1 or S2 is known, and the semiconductor layer is not fully depleted, then the buried oxide thickness can be determined from the measured minimum high frequency capacitance. Second, the buried oxide thickness can be determined from the measured maximum low-frequency capacitance, which is equal to the buried oxide capacitance. Third, if the conductivity type of S1 and S2 is not the same, then the oxide thickness can be determined from the measured maximum high-frequency capacitance [45]. The fixed oxide charge density can be determined from the voltage shift of high frequency C-V curve by comparing the experimental curve with the ideal C-V curve. By applying a gate bias to accumulate at one interface gives the fixed oxide charge at the other interface. Therefore, Q_{f1} and Q_{f2} can be determined independently in different parts of the measured C-V curve.

If the buried oxide thickness is known, then the doping concentrations in S1 and S2 can be estimated from the minimum high-frequency capacitance regardless of the interface trap density [45]. However, the layer thickness in S1 is usually thin enough

to be completely depleted before reaching its capacitance minimum, and hence the buried oxide thickness can not be determined from the high frequency minimum capacitance. Therefore, an independent characterization method is needed to determine the doping concentration before the layer is fully depleted. In analogy to the MOS theory [46] the doping concentration of a SIS capacitor can be determined by

$$N_{d2}(w_2) = -2\left\{q\epsilon_s \frac{d}{dV_G}\left[\frac{1}{(1-K_2)C_{HF}^2}\right]\right\}^{-1} \tag{3.34}$$

where ϵ_s is the dielectric permittivity, and w_2 is the distance from the substrate/oxide interface. It is noted that $(1-K_2)$ can not be determined without knowing the doping concentrations in S1 and S2. However, this can be solved by using iteration procedure. A rapid convergence is expected, since $(1-K_2)$ is relatively insensitive to the doping concentration, especially near the midgap.

3.7 Results and Discussion

The starting material was n-type, 3-5 Ω-cm Czochralski grown silicon wafers. The wafer temperature was maintained at 550°C during oxygen implantation. The implant energy was 150 KeV and the oxygen dose was 1.8×10^{18} cm^{-2}. The SIMOX wafers were then annealed at 1285°C for 2 hours in an N_2/O_2 ambient. An n-type epilayer was then grown on the SIMOX substrate. Finally, an n^+ layer was created for ohmic contacts. The capacitance and conductance measurements were performed on these SIS capacitors using a HP 4192A impedance analyzer. The SIS capacitor structure and a typical high-frequency (1 MHz) C-V curve measured at room temperature are shown in Fig. 3.9.

By neglecting the voltage stretchout caused by interface traps, doping concentrations at S1 and S2 are determined from the slope of $1/[(1-K_2)C_{HF}^2]$ plot, which gives $N_{d1} = 5.0 \times 10^{15}$ cm^{-3} and $N_{d2} = 1.8 \times 10^{15}$ cm^{-3}. Figure 3.10 shows the apparent and corrected $1/C^2$ versus V_G curves. It is clearly shown that neglecting the coupling factor can lead to an erroneous result. The doping concentration in S2 determined

from the minimum high-frequency capacitance (Fig. 3.9) gives the same value as is determined by the slope shown in Fig. 3.10, but overestimates by a factor of 2 in S1, indicating a fully depleted film at $V_G \approx 5$ V. The buried oxide layer thickness is determined from the measured minimum high-frequency capacitance in S2, which yields $t_{ox} = 362$ nm. Fixed oxide charge densities determined by the voltage shift of the C-V curve in weak inversion yielding value of $Q_{f1}/q = 1.9 \times 10^{11}$ cm^{-2} and $Q_{f2}/q = 1.2 \times 10^{10}$cm^{-2}, respectively.

High-low frequency capacitance method has been shown to be a useful tool for analyzing the interface properties of a MOS capacitor. However, in a SIMOX SIS capacitor, the leakage current is generally larger than that of a thermally oxidized MOS capacitor. Thus, for low-frequency C-V measurement, losses in the buried oxide measured at room temperature can not be neglected. It is usually tedious and difficult to account for these losses. Instead, we use a "high-frequency" quasi-static C-V method to obtain the quasi-static C-V curve. The measurement is performed under external excitation (heat or light), to reduce the minority carrier response time. Thus, quasi-static condition can be easily satisfied at a relatively high measurement frequency. Figure 3.11 shows the quasi-static (7 kHz) and high-frequency (1 MHz) C-V curves measured at 425 K. In the quasi-static C-V curve, the two valleys correspond to depletion in S1 and S2. The buried oxide thickness is calculated from the maximum low-frequency capacitance data, which yields $t_{ox} = 366$ nm. The thickness of the buried oxide obtained from the maximum low-frequency capacitance is within 2 % of that obtained from the minimum high-frequency capacitance data. The interface trap densities are determined from (3.13) by comparing the quasi-static and high-frequency C-V curves measured at 425 K, and the surface potential versus gate bias is determined by solving (3.33).

Conductance measurements were carried out at room temperature using impedance analyzer. Figure 3.12 shows the measured conductance-voltage curves for f = 100 kHz

and 1 MHz. Two conductance peaks correspond to depletion in S1 and S2. The conductance as a function of gate bias goes through a peak, indicating that the loss is predominantly caused by interface traps rather than by the bulk traps. With increasing frequency, the peaks shift towards flat-band voltage and tend to merge into a single peak. This means that, at high frequencies, the interface trap loss from S1 and S2 will interact with one another. Consequently, the extraction of the interface trap parallel admittance will be erroneous in this region if the coupling factor is not taking into account. Figures 3.13 and 3.14 show G_p/ω in S1 and S2 as a function of frequency with V_G as a parameter. The interface trap density D_{it} and the capture cross section σ_n can be determined from the magnitudes and positions of the G_p/ω peaks. This is done by using the continuum interface state model. Also, the interface trap density profile $D_{it}(E)$ can be constructed after determining the surface potential as a function of the gate voltage. This is obtained by using high-frequency capacitance method. Figures 3.15 and 3.16 summarize the interface trap density profiles determined by the capacitance and conductance methods applied to S1 and S2, respectively. Interface trap capture cross sections σ_n determined by the conductance method for the S1 and S2 are shown in Fig. 3.17.

It is shown, from the capacitance and conductance measurements, that both interface trap densities increase toward the band edge with a minimum near midgap, similar to that observed in thermally grown oxide. The midgap interface trap density at the F/O interface is approximately an order of magnitude higher than that observed at the S/O interface. Note that the extremely high oxygen fluence required to form a buried oxide layer in silicon by ion implantation coupled with the extremely reactivity of the ion beam lead one to speculate that a significant concentration of metal impurities may be incorporated into silicon film during implantation. High midgap interface trap density at the F/O interface observed in our study suggests the possibility of gettering the metal contaminants by the structure defects near the

F/O interface. This gettering process tends to increase their electrical activity, leading to increased interface trap density. The discrepancy between the interface trap densities determined by the capacitance and conductance methods can be reduced by using the statistical model of Nicollian and Goetzberger [50] which accounts for surface potential fluctuations. The discrepancy can also be caused by the different measurement temperatures used in the capacitance and conductance methods.

3.8 Conclusion

In summary, a model for electrical characterization of the SIMOX SIS capacitor has been derived. By introducing a coupling factor, we were able to reduce the equivalent circuit of a SIS capacitor to a MOS-like equivalent circuit. Thus, the existing MOS capacitor characterization methods can be applied directly to a SIS capacitor. Expressions for determining the interface trap densities from the capacitance and conductance methods were derived, which contained an extra correction factor as compared to that of the conventional MOS theory. Determination of the surface potential as a function of gate bias requires a combination of theoretical calculations, and low- or high- frequency capacitance methods. The results indicate that midgap interface trap density determined by the conductance method is about $2 \sim 3 \times 10^{10}$ $cm^{-2}eV^{-1}$ at the S/O interface and $2 \sim 3 \times 10^{11}$ $cm^{-2}eV^{-1}$ at the F/O interface. Interface trap densities at both interfaces increase toward band edge, similar to that observed in thermally grown oxide. As was pointed out previously [52,53] the semiconductor nature of the back gate of SOI MOSFET's should be taken into account in device modeling. The present model enables one to use the capacitance and conductance methods for analyzing the interface properties in SOI materials.

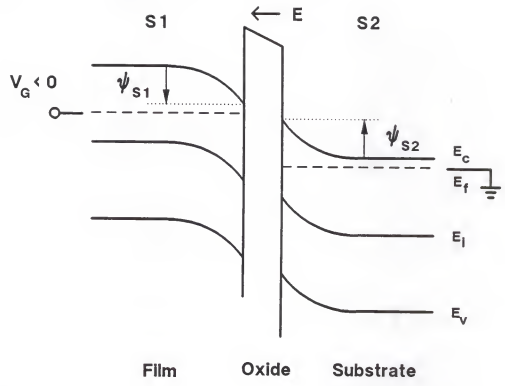

Figure 3.1 Energy band diagram of an n-i-n semiconductor-insulator-semiconductor structure.

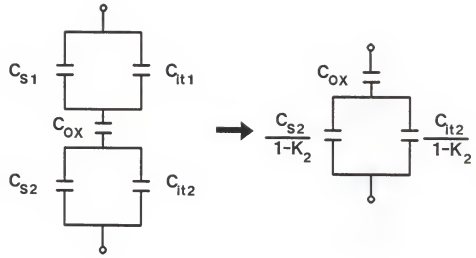

Figure 3.2 Simplified small signal equivalent circuit for a SIS capacitor and its MOS-like equivalent circuit.

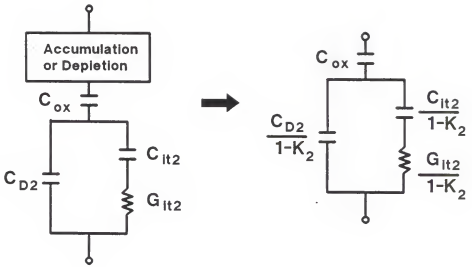

Figure 3.3 Simplified small signal equivalent circuit of a SIS capacitor in depletion for a single-level interface trap and its MOS-like equivalent circuit.

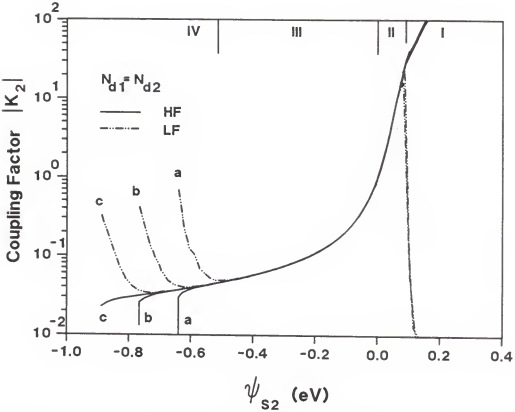

Figure 3.4 Coupling factor as a function of surface potential in an n-i-n SIS structure with equal doping concentration in both semiconductors as a parameter. t_{ox} = 350 nm and $N_{d1} = N_{d2}$ = (a) 10^{15}, (b) 10^{16}, and (c) 10^{17} cm^{-3}. Interface state density and fixed oxide charge density are assumed zero in S1 and S2.

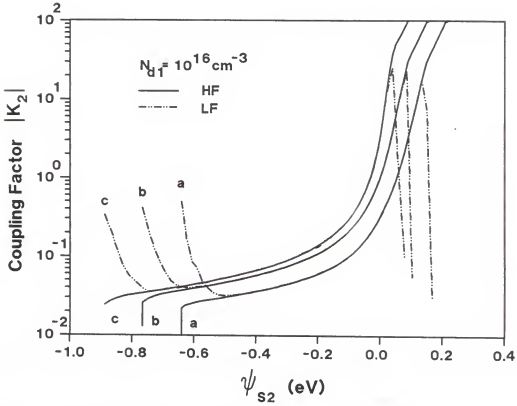

Figure 3.5 Coupling factor as a function of surface potential for an n-i-n SIS structure with doping concentration in semiconductor 2 as a parameter. t_{ox} = 350 nm, $N_{d1} = 10^{16}$ cm^{-3}, and N_{d2} = (a) 10^{15}, (b) 10^{16}, and (c) 10^{17} cm^{-3}. Interface state density and fixed oxide charge density are assumed zero in S1 and S2.

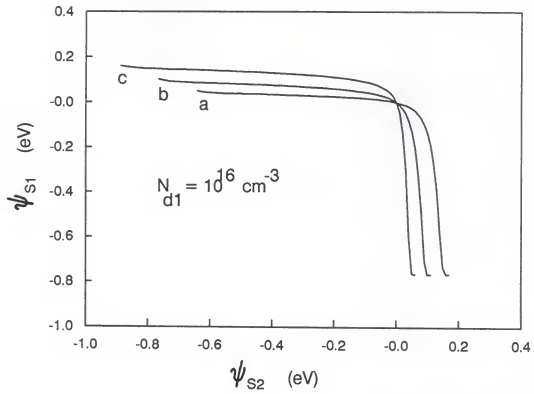

Figure 3.6 Surface potential ψ_{s1} as a function of ψ_{s2} with doping concentration in semiconductor 2 as a parameter. t_{ox} = 350 nm, $N_{d1} = 10^{16}$ cm^{-3}, and N_{d2} = (a) 10^{15}, (b) 10^{16}, and (c) 10^{17} cm^{-3}. Interface state density and fixed oxide charge density are assumed zero in S1 and S2.

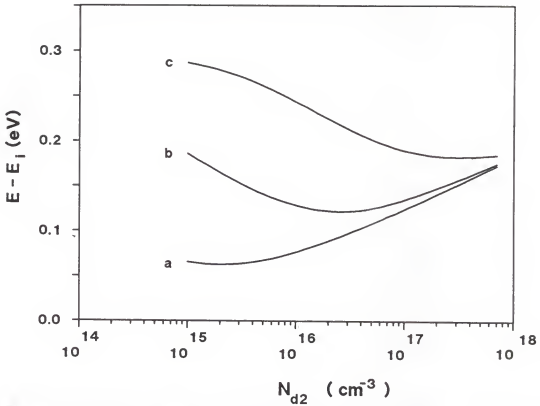

Figure 3.7 The region where MOS theory is applicable to a SIS capacitor, $|K_2| < 0.1$, as a function of N_{d2} with N_{d1} as a parameter. $t_{ox} = 350$ nm and $N_{d1} =$ (a) 10^{15}, (b) 10^{16}, and (c) 10^{17} cm^{-3}. Interface state density and fixed oxide charge density are assumed equal to zero in S1 and S2.

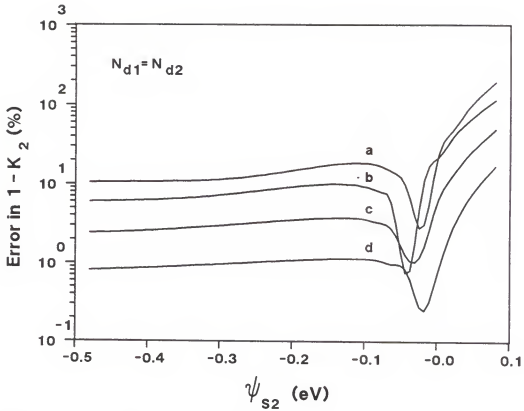

Figure 3.8 The error (in percent) between $1-K_2$ and $1-K_2'$ as a function of surface potential. $t_{ox} = 350$ nm, $D_{it1} = D_{it2} = 5 \times 10^{11}$ $cm^{-2}eV^{-1}$ and $N_{d1} = N_{d2}$ = (a) 10^{15}, (b) 10^{16}, (c) 10^{17}, and (d) 10^{18} cm^{-3}. Fixed oxide charges are assumed zero in S1 and S2.

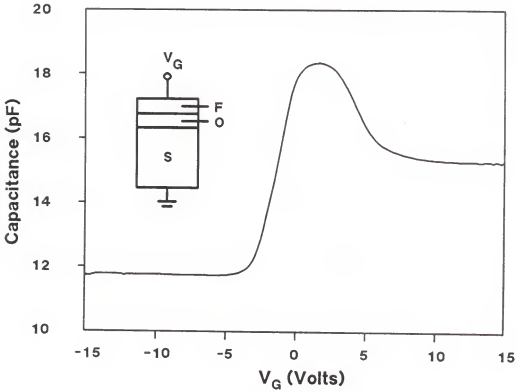

Figure 3.9 Typical 1 MHz C-V curve measured at room temperature and basic experimental structure, where F is the top silicon film, O is the buried oxide layer, and S is the substrate.

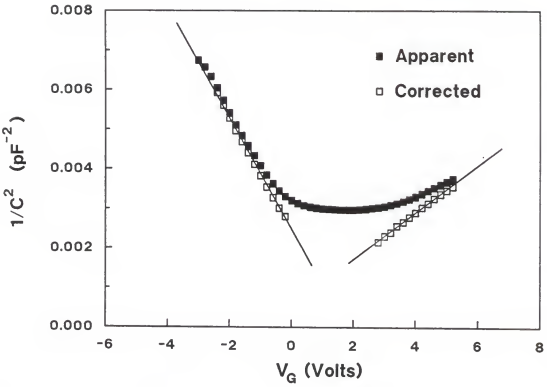

Figure 3.10 Apparent and corrected $1/C^2$ versus gate bias curves deduced from Fig. 3.9. Approximated coupling factor K_2' is used in the correction.

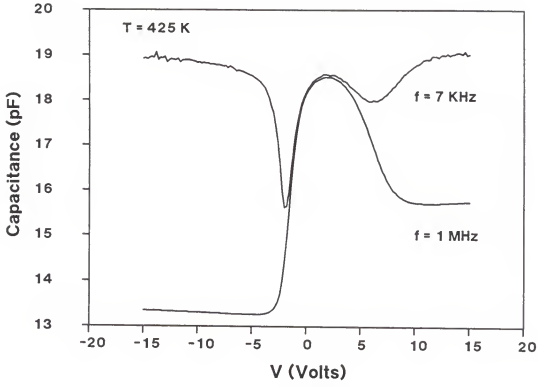

Figure 3.11 The quasi-static and high frequency C-V curves measured at 425 K.

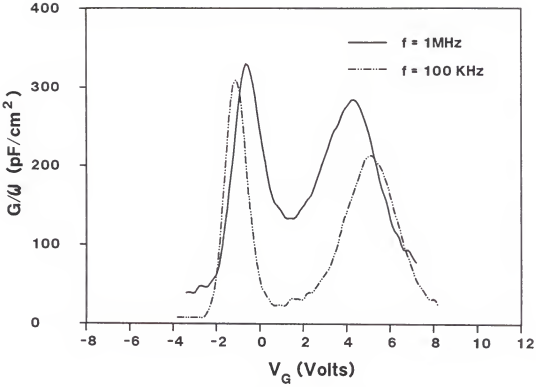

Figure 3.12 The measured conductance versus gate voltage for f = 100 kHz and 1 MHz.

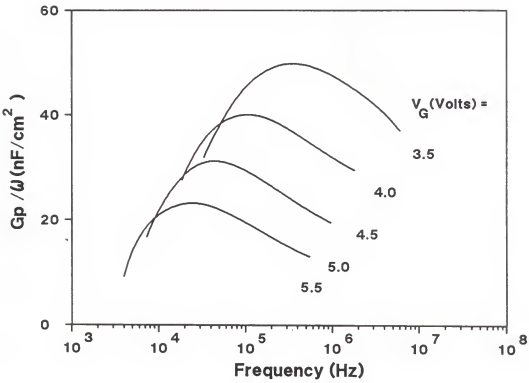

Figure 3.13 Experimental G_p/ω versus frequency curves for various gate voltages at the film/oxide interface.

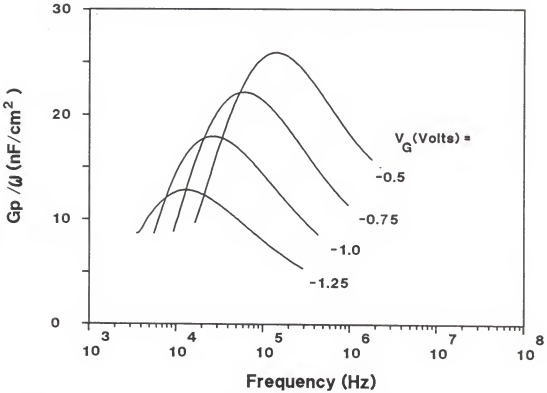

Figure 3.14 Experimental G_p/ω versus frequency curves for various gate voltages at the substrate/oxide interface.

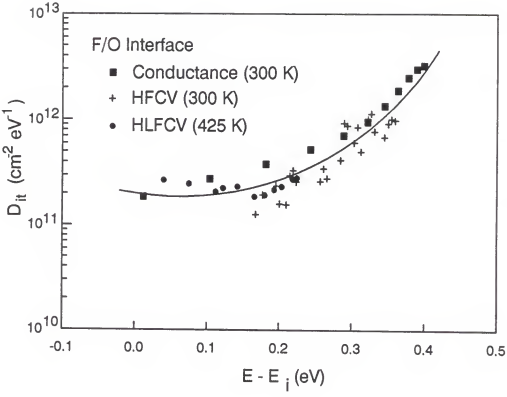

Figure 3.15 Interface state profile determined by high frequency C-V (HFCV), high-low frequency C-V (HLFCV), and conductance methods at the film/oxide interface.

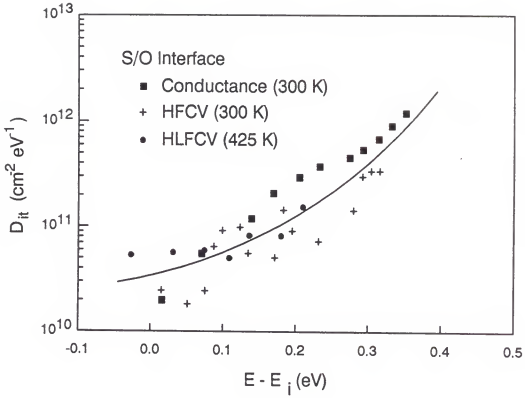

Figure 3.16 Interface state profile determined by high frequency C-V (HFCV), high-low frequency C-V (HLFCV), and conductance methods at the substrate/oxide interface.

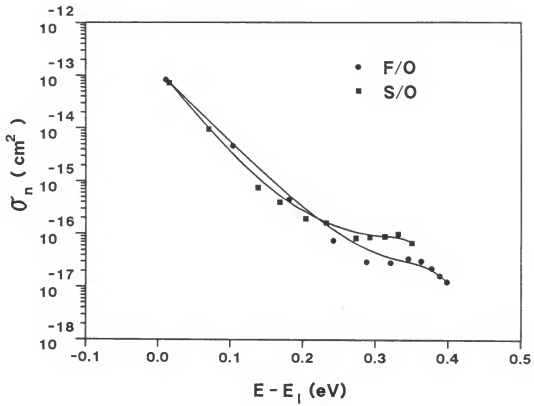

Figure 3.17 Interface state capture cross sections versus energy determined by the conductance method at the film/oxide and the substrate/oxide interfaces.

CHAPTER 4
A MODEL FOR ANALYZING THE INTERFACE PROPERTIES OF A SEMICONDUCTOR-INSULATOR-SEMICONDUCTOR STRUCTURE: TRANSIENT CAPACITANCE TECHNIQUES

4.1 Introduction

Deep-level transient spectroscopy (DLTS) has been extensively used to study the energy levels and capture cross sections of bulk traps in a p-n junction diode and the interface traps of a MOS capacitor. However, conventional DLTS measurements using these test structures on the SIMOX substrate have been shown to be difficult to obtain accurate information concerning bulk traps and interface states in the top silicon film due to large series resistance [54]. To overcome this problem, SOI MOSFET's has been used for the conductance or current DLTS measurement to determine the bulk traps in the top silicon film [55,56]. Due to high densities of bulk traps and interface states at both the front and back gates of SOI MOSFET's, it is difficult to differentiate between the bulk defects and the interface traps. McLarty et al. [39] have applied suitable bias at both the front and back gates to obtain useful information of bulk traps in the top silicon film. However, no information about the substrate/buried oxide interface was reported.

To analyze the trapping properties of interface states that are continuously distributed in the energy bandgap encounters some difficulties since the DLTS signals are contributed by continuous interface traps with different capture cross sections and different activation energies. Furthermore, bulk traps and generation-recombination centers also exist in SOI substrates which makes distinction among these different sources of transient signals a very complex task. To overcome these difficulties, Johnson and Wang [57,58] proposed an energy resolved DLTS technique. Katsube and

Kakimato [59] have discretized the distributed interface states by applying small trap filling pulses leading to improved energy resolution. Yamasaki et al. [60] have separated bulk traps and interface states by applying different pulse voltages. Kumar and Iyer [61] introduced DLTS with bias scanning at a fixed temperature instead of the commonly used temperature scan at a fixed bias.

Based on the model described in Chapter 3, we employ small trap filling pulse bias-scan DLTS technique, suitable for MOS structure, to analyze the interface traps at both the F/O and S/O interfaces of a SIMOX SIS capacitor, and to present a simple method for differentiating among transient signals caused by bulk traps, interface states, and minority carrier generation. Furthermore, we show that under proper bias condition the charges at the top silicon film can be decoupled from the underlying substrate. Therefore, conventional temperature-scan DLTS and Zerbst methods can be directly applied to a SIS capacitor without taking the charge coupling factor into account.

4.2 Bias-Scan DLTS Technique

It seems difficult to use DLTS technique on a SIS capacitor, since this technique involves carrier dynamics at both the F/O and S/O interfaces. Also, bulk traps and recombination-generation centers in a SIS capacitor further complicate the analysis. We shall show later that with some modification, the MOS capacitor theory can be applied to a SIS capacitor if the interface to be characterized is kept from strong accumulation. In this section we employ a bias-scan DLTS technique [61,63] on a SIS capacitor to achieve energy resolution with simple interpretation. In this technique, a small trap filling pulse is applied as the quiescent bias is scanned at a fixed temperature and a fixed rate window. As the Fermi level scans across the bandgap, a peak in the DLTS signal is obtained when the emission time constant of the surface states in a small energy interval of the forbidden gap matches the rate window. The surface potential corresponding to the bias at peak DLTS signal is used to determine

the energy of the interface states. By varying the rate window or, equivalently, the temperature of measurement yields direct information concerning the interface state distribution. The capture cross section is obtained by using the detailed balance relation, while the energy level is independently determined from the surface potential. Therefore, it is essential to know the surface potential as a function of applied bias at the measurement. The capacitance-voltage method discussed in Chapter 3 is used to obtain the buried oxide capacitance and doping density.

4.2.1 Carrier Dynamics of the SIS Capacitor

Figure 4.1 illustrates the sequences of the trap filling pulse, the capacitance change observed and the energy band bending of an n-Si/SiO_2/n-Si (n-i-n) SIS capacitor with substrate grounded and a quiescent gate bias V_G applied to the top silicon film. For simplicity, we shall refer to the top silicon film as semiconductor 1 (S1), the substrate as semiconductor 2 (S2), and the subscript 1 or 2 as the parameters of S1 or S2. Since the substrate is grounded, $V_G > 0$ depletes the F/O interface and $V_G < 0$ depletes the S/O interface. In the case of moderate fixed oxide charge, it is generally true that if one interface is in depletion the other interface will be in accumulation. In the following analysis, we consider the case of a "positive" filling pulse superimposed on a negative quiescent bias which tends to characterize the S/O interface. Similar analysis applies to a "negative" filling pulse superimposed on a positive gate bias for the characterization of the F/O interface. Applying a positive filling pulse to a SIS capacitor fills the states below the Fermi level at the S/O interface and empties the states above the Fermi level at the F/O interface ($t_0 < t < 0$). At the end of the pulse ($t = 0$), the S/O interface starts to emit the captured carriers and the F/O interface tends to fill the empty interface states below the Fermi level.

The transient capacitance signals consist of both carrier capture and emission at the F/O and S/O interfaces of a SIS capacitor. The capture process at the F/O interface for is assumed to be an exponential function of time with a characteristics

filling time constant [64]

$$\frac{1}{\tau_c} = \sigma_n v_{th} n + e_n + e_p \tag{4.1}$$

where e_n (e_p) is the electron (hole) emission rate, σ_n is the electron capture cross section, v_{th} is the thermal velocity, and n is the free-electron concentration.

The characteristic filling time constant τ_c can be estimated from (4.1). For example, with $\sigma_n v_{th} n \gg e_n$ and e_p, $\sigma_n = 10^{-15}$ cm^2, $v_{th} = 1.2\times10^7$ cm/s, and $n = 10^{15}$ cm^{-3}, yields $\tau_c = 83$ ns. Note that $n = 10^{15}$ cm^{-3} is used in the calculation, which ensures this capture process is even shorter when the F/O interface is in accumulation with $n > 10^{15}$ cm^{-3}. This characteristic filling time is much smaller than the sampling times t_1 and t_2 of the selected rate windows. Therefore, the measured capacitance transients will not be affected by the presence of F/O interface states, due to their rapid capture of electrons under the prevailing accumulation of the F/O interface. The accumulated F/O interface has no influence on the slow capacitance transient caused by carrier emission from the S/O interface. This implies that the measured capacitance transient ΔC is dominated by carrier emission from the S/O interface.

When a small quiescent bias is applied, the F/O interface can be driven into depletion instead of accumulation. Therefore, slow carrier capture transient due to lack of free carriers in the F/O interface will be encountered. Such a slow capture process will change the carrier capture time from nanosecond range to microsecond range or higher depending on the gate bias applied. When the sampling times t_1 and t_2 are comparable to the carrier capture time, DLTS signals will be a combination of the two sources, namely, the carrier emission from the S/O interface and carrier capture at the F/O interface. Under this condition, no useful information about defect parameters can be obtained. It is easy to identify this condition, since capture of the majority carriers gives a positive capacitance transient $\Delta C > 0$, and emission of the majority carriers gives a negative capacitance transient $\Delta C < 0$.

4.2.2 Bias-Scan DLTS Analysis

In the bias-scan DLTS measurement, the surface of the S/O interface is always kept in depletion or weak accumulation to avoid minority carrier generation or slow carrier capture at the F/O interface. A small positive pulse ΔV is then applied to the film in superposition to the quiescent bias voltage, so that the S/O interface is driven into depletion, while the F/O interface is driven into accumulation during the filling pulse. By quickly returning the bias voltage to its quiescent value after the interface states located below the Fermi level are filled with electrons, the electrons are emitted from the filled traps above the Fermi level with characteristic emission rate that depends exponentially on temperature. In the F/O interface, the electrons are captured by the emptied traps located below the Fermi level. The electron transition between the interface states and the conduction band results in a capacitance transient which is sampled at time t_1 and t_2. Since the variation of capacitance transient from the film will not be detected due to its rapid carrier capture, the variation of capacitance simply represents the change of depletion layer width at the substrate. Assuming that ΔC is much smaller than the total capacitance C_T, one obtains the following approximation [61]

$$\Delta C \approx -\frac{C_{so}^3}{q\epsilon_s N_{d2} C_{ox}} \int_{E_v}^{E_c} S[e_n(E)] \cdot D_{it2}(E) \cdot (f_1 - f_2) \cdot dE \tag{4.2}$$

where

$$S[e_n(E)] = \exp[-e_n(E)t_1] - \exp[(-e_n(E)t_2] \tag{4.3}$$

$$\frac{1}{C_{so}} = \frac{1}{C_{ox}} + \frac{1}{C_{s2}} \tag{4.4}$$

C_{ox} is the buried oxide capacitance, C_{s2} is the surface capacitance, N_{d2} is the donor density, and

$$f_1(E) = 1 - \left[1 + \exp\left(\frac{E - E_F}{kT}\right)\right]^{-1} \tag{4.5}$$

and

$$f_2(E) = 1 - \left[1 + \exp\left(\frac{E - E_F + \Delta E}{kT}\right)\right]^{-1} \tag{4.6}$$

are electron occupation functions of the surface states at the quiescent bias and during the filling pulse, respectively. Figure 4.2 shows $(f_1 - f_2)$ as a function of energy with variation of surface potential ΔE caused by a small trap filling pulse ΔV, as a parameter. The integral in (4.2) is evaluated at the states with energy level E_T to obtain [61]

$$\Delta C \approx -\frac{C_{so}^3}{q\epsilon_s N_{d2} C_{ox}} D_{it2}(E_T) S[e_n(E_T)] \alpha(\Delta E) \beta(\Delta E) \tag{4.7}$$

where α is the height and β the full width at half maximum of the $(f_1 - f_2)$ function for a given filling pulse height.

The energy of the interface trap is obtained from the surface potential corresponding to the peak of bias-scan DLTS signal which can be determined by high-frequency capacitance-voltage measurements as described in Chapter 3. The capture cross section can be obtained from the detailed balance relation

$$e_n = \sigma_n v_{th} N_c \exp\left(-\frac{E_c - E_T}{kT}\right) \tag{4.8}$$

where N_c is the effective density of states in the conduction band. The emission rate at the peak DLTS signal is determined by the rate window, $\ln(t_2/t_1)/(t_2 - t_1)$. The DLTS signal of (4.7) has a maximum when the emission rate matches the rate window. When the rate window or the temperature is varied, the peaks occur at different positions of the Fermi level in the band gap. Thus, a direct map of interface state distribution is obtained.

In the case of high-frequency operation, the frequency is high enough so that the interface traps can not follow the a.c. signal. Therefore, $C_{it2} = 0$ and (3.9) reduces to the following expression:

$$\frac{1}{C_T} = \frac{1}{C_{ox}} + \frac{1 - K_2}{C_{s2}} \tag{4.9}$$

where the high-frequency coupling factor is defined by $K_2 \equiv -(C_{s2}/C_{s1})$. By rearranging (4.9), we can express C_{so}, in terms of the measurable quantities, as

$$C_{so} = (1 - K_2)\left(\frac{1}{C_T} - \frac{K_2}{C_{ox}}\right)^{-1} \tag{4.10}$$

Therefore, the interface state density can be readily determined from the measured capacitance using (4.7).

Capacitance-voltage and gate bias versus surface potential curves are shown in Fig. 4.3. Doping concentrations and buried oxide thickness of the SIMOX SIS capacitor are determined by using high-frequency C-V method which gives $N_{d1} = 5 \times 10^{15}$ cm^{-3}, $N_{d2} = 1.8 \times 10^{15}$ cm^{-3}, and $C_{ox} = 362$ nm. Surface potential versus gate bias is calculated by using modified Terman's method. Bias-scan DLTS measurements were performed at selected temperatures and rate windows. Figures 4.4 and 4.5 show the DLTS signals as a function of the bias voltage for different sample temperatures and rate windows at the F/O and S/O interfaces, respectively. A small filling pulse height of 100 mV and a pulse width of 1 ms were used in the DLTS measurements.

A slow d.c. bias ramp rate was used to eliminate any hysteresis between forward and reverse ramp directions. As the temperature is lowered, the emission time constants of all the states are reduced; hence to find the states having a particular emission time, one needs to explore the states closer to the conduction band edge, as is shown in Fig. 4.4. Similarly, if a faster rate window is selected for a fixed temperature measurement, to find the state matches the rate window, one needs to use small quiescent bias to explore the states closer to the conduction band edge, as is shown in Fig. 4.5.

The transient capacitance signals in a MOS or SIS capacitor consist of bulk trap, interface state, and minority carrier generation. Due to high densities of bulk defects and interface states in the SIMOX wafer, minority carrier generation is significant within the observed transient time in the conventional large pulse DLTS measurements on a SIS capacitor. In bias-scan DLTS technique, the minority carrier generation can be neglected since the Fermi level is always kept above midgap. Also, this process can be suppressed by performing the measurement at a lower temperature. The strong temperature dependence of minority carrier generation is shown in

Fig. 4.6. When the temperature is decreased from 300 to 220 K, the minority carrier generation process is significantly suppressed.

Bulk traps in SIMOX wafers generally consist of discrete energy levels [39,56]. Since the bias-scan DLTS measurements are performed at a fixed temperature, the emission rate for the discrete level is fixed which results in a constant shift of the base line in the DLTS signal. This can be easily distinguished from the contribution of interface states. If the discrete level is spatially nonuniform and dominant over interface states, the bias-scan DLTS is similar to the techniques used in the bulk defect profiling [62]. Since variation of the bias voltage is proportional to the change of depletion edge, the peak position of the DLTS signal caused by bulk trap should be independent of the rate window or temperature used in the measurement. Therefore, bulk trap can be easily distinguished from the rate window or temperature dependent interface state signal. Indeed as shown in Figs. 4.4 and 4.5, the peak position changes with quiescent bias, since interface states of different energies are being sampled. It is also noted that the base lines of the bias-scan DLTS signals shown in Figs. 4.4 and 4.5 are much smaller than the transient signals from the interface states at both the F/O and S/O interfaces, indicating the transient signals from the bulk traps are not significant for the selected rate windows and temperatures in these measurements. This result is also consistent with our conductance measurements.

The interface state distributions at the F/O and S/O interfaces obtained from the bias-scan DLTS and the conductance methods are shown in Fig. 4.7. Note that the density of midgap states of the F/O interface was about an order of magnitude higher than that of the S/O interface. On the average, the interface trap density determined by the bias-scan DLTS was slightly smaller than that determined by the conductance method. This discrepancy is especially significant when the interface trap density is nonuniformly distributed across the bandgap. Such a discrepancy can be caused by the different approximations used in the DLTS and conductance methods. It is

also interesting to note the difference between these two methods. In the conductance method G_p/ω versus frequency (with bias as a parameter) will spread over a frequency range determined only by the time constant dispersion [50]. However, in the bias-scan DLTS, ΔC versus bias (with rate window or temperature as a parameter) will spread over a bias range determined by the time constant dispersion and the density of interface states. Since the interface states are more uniformly distributed across the bandgap in the F/O interface, as is shown in Fig. 4.7, the agreement of these two methods at the F/O interface is better than that at the S/O interface. To eliminate the spreading caused by the nonuniform interface states, correlation DLTS [63,64] can be used, and ΔC is measured as a function of time constant of the exponential decay weighting function with bias as a parameter.

In SIMOX wafers, defects created within or near the interfacial region are due to dislocations, oxygen precipitates, and various metal impurities during oxygen implantation. The results of our study reveal that the energy distribution of both interface state densities at the F/O and S/O interfaces increase toward the band edge with a minimum occurring near midgap, similar to that observed in thermally grown oxide. Since there is a correlation between the microstructure roughness and the electrical defect density at the SiO_2 interface [40], it is not surprising to observe higher interface trap densities at the F/O interface than that at the S/O interface. The structure defects can also getter metal impurities introduced during oxygen implantation which resulted in an increase of their electrical activity. Our results show that the midgap interface trap density is about $2 \sim 3 \times 10^{11}$ $cm^{-2}eV^{-1}$ at the F/O interface and $2 \sim 3 \times 10^{10}$ $cm^{-2}eV^{-1}$ at the S/O interface. It is possible to determine the capture cross section of electrons using the detailed balance relation. Values of capture cross sections at the F/O and S/O interfaces determined by this method in our SIMOX samples are found to be $10^{-14} \sim 10^{-16}$ cm^2.

4.3 C-t and Temperature-Scan DLTS Techniques

4.3.1 Decoupling at the F/O and S/O Interfaces

It is shown that the total capacitance of a SIS capacitor can be reduced to a MOS-like capacitor by

$$\frac{1}{C_T} = \frac{1}{C_{ox}} + \frac{1 - K_2}{C_{s2} + C_{it2}} \tag{4.11}$$

The coupling factor $K_2 = -(C_{s2} + C_{it2})/(C_{s1} + C_{it1})$ takes into account the charge coupling between the film and the substrate. If $K_2 = 0$, then the equivalent circuit of a SIS capacitor will reduce to the conventional MOS equivalent circuit. Figure 4.8 shows the typical C_{s1}, C_{s2}, C_{ox} and C_T of a SIS capacitor versus gate voltage. If the substrate is biased into strong inversion, the film will be in accumulation with $C_{s1} \gg C_{s2}$. In this case, the total capacitance will be simply a series combination of C_{ox} and C_{s2}, i.e., a MOS capacitor. The measured capacitance transients will not be affected by the presence of F/O interface states, due to their rapid capture of electrons under the prevailing accumulation of the F/O interface. The condition for fast carrier capture at the F/O interface can be easily satisfied by pulsing the S/O interface into deep depletion which will cause accumulation at the F/O interface. Under this bias condition, a SIS capacitor can be treated as a simple MOS capacitor. Therefore, C-t and DLTS can be directly applied to a SIS capacitor.

4.3.2 C-V and C-t analysis

The starting material was n-type, 3-5 Ω-cm Czochralski grown silicon wafers. The wafer temperature was maintained at 550°C during oxygen implantation. The implant energy was 150 KeV and the oxygen dose was 1.8×10^{18} cm^{-2}. The wafers were then annealed at 1150°C for 3 hours or 1250°C for 2 hours in a nitrogen ambient, respectively.

The results of our analysis of the C-V, C-t, and temperature-scan DLTS data are summarized in Table 4.1. The buried oxide thickness t_{ox} can be determined from the measured maximum quasi-static capacitance, which is equal to the buried-oxide capacitance. Once the buried oxide thickness is determined, N_{d1} and N_{d2} are

estimated from the minimum high-frequency capacitance [45]. The high-frequency capacitance measured in the dark and the quasi-static capacitance measured under strong illumination are shown in Fig. 4.9. Although the quasi-static C-V curve is made at a frequency of 7 kHz, the quasi-static condition is satisfied under strong illumination. In the quasi-static C-V curve, the two valleys correspond to depletion in the film and the substrate, respectively. As the annealing temperature rises, the buried oxide thickness also increases. This suggests that during the post implantation annealing, most of the oxygen atoms released by oxygen precipitates diffused toward the F/O interface [37]. The increase of N_{d1} at lower anneal temperatures has also been reported [65], and is related to oxygen donor complexes (thermal donors) and SiO_x precipitates (new donors).

C-t analysis is based on the measurements of capacitance transient caused by pulsing an interface from accumulation into deep depletion. This condition eliminates transients arising from the other interface and ensures that the charge coupling at both interfaces is negligible. Figure 4.10 shows the C-t response at the film and the substrate of the SIS capacitors receiving different post implantation annealing. The time required for the capacitance to change from its initial value to the final value $C_T(t_F)$ is $t_F \sim 8$ s for the substrate and $t_F < 0.1$ s for the film. A comparison of C-t transients of Fig. 4.10 shows that the relaxation times of the substrate are two to three orders of magnitude longer than the relaxation times for the film. By comparing the devices with different anneal temperatures, it is shown that t_F is increased by a factor of 10 at the film for the samples annealed at 1250 °C. However, no significant improvement was observed in the substrate.

The generation lifetime τ_g is related to the slope of Zerbst plot shown in Fig. 4.11 by [46]

$$-\frac{d}{dt}\left[\frac{C_{ox}}{C_T(t)}\right]^2 = \frac{2n_i}{\tau_g N_d}\frac{C_{ox}}{C_T(t_F)}\left[\frac{C_T(t_F)}{C_T(t)} - 1\right] \qquad (4.12)$$

It should be pointed out that the existence of a linear region in the Zerbst plot

implies that the generation of minority carriers is proportional to the depletion layer width. Similar Zerbst plots were also observed in the film. Note that value of τ_{g1} ($\sim 0.2\mu s$) obtained at the 1250°C, 2 hrs annealed samples is comparable to that reported previously for the recrystallized SOI wafers [66].

4.3.3 Temperature-Scan DLTS Analysis

For electron emission from a continuous distribution of interface states, the DLTS signal ΔC is given by [60]

$$\Delta C \approx -\frac{kTC_T^3}{q\epsilon_s N_d C_{ox}} D_{it}(E) \cdot \ln\left(\frac{t_2}{t_1}\right) \tag{4.13}$$

where q is the electronic charge, ϵ_s is the permittivity of silicon, k is Boltzmann's constant, and T is the absolute temperature. If the electron capture cross section is not strongly dependent on energy, then the DLTS signal is peaked at an emission rate given by $e_n = (t_2 - t_1)^{-1}\ln(t_2/t_1)$ which corresponds to an energy (relative to midgap)

$$E = \frac{E_g}{2} - kT \cdot \ln\left[\frac{\sigma_n v_{th} N_c (t_2 - t_1)}{\ln(t_2/t_1)}\right] \tag{4.14}$$

where E_g is the bandgap energy and N_c is the effective density of states of the conduction band. Therefore, the temperature scan of the DLTS signals is directly related to the energy distribution of the interface state density, namely, T and $\Delta C/T$ are proportional to E and D_{it}, respectively.

Figures 4.12 and 4.13 show the DLTS spectra of the F/O and the S/O interfaces for samples processed identically except for the post implantation annealing. The DLTS spectra were obtained by biasing the SIS capacitor into deep depletion, and periodically pulsing the gate voltage into accumulation in order to populate both the interface states and the deep levels in the depletion layer. The DLTS signal at low temperatures corresponds to states near the conduction band edge while the signal at higher temperature measures states near the midgap. The rapid drop in the DLTS signal at temperatures below $\sim$ 120 K may arise from a dependence of the capture

cross section on energy near the conduction band edge. The rise in the DLTS signals above 250 K is ascribed to the onset of minority carrier generation. The analysis is applicable over the region of the spectrum where the signal is dominated by electron emission and the capture cross section is assumed to be a constant. The interface state distribution at midgap cannot be determined from the DLTS measurements due to the onset of minority carrier generation at high temperatures. Figures 4.14 and 4.15 show the interface state distribution obtained from the DLTS measurements. The interface state profiles calculated using $\sigma_n = 10^{-15}$ cm^2 show that D_{it} is in the range of $10^{10} \sim 10^{12}$ cm^{-2}eV^{-1} and increases toward the conduction band edge. Note that a decrease of σ_n by an order of magnitude causes only the shift of D_{it} curves towards the conduction band edge by 2.3 kT.

As shown in Table 4.1, increasing anneal temperature tend to increase τ_g and decrease D_{it} at both the film and the substrate. This tendency is more pronounced at the film than at the substrate. This effect is due to annealing out of precipitates and dislocations, as well as a sharpening of the buried oxide interfaces [3,38]. The slight hump around $E_i + 0.2$ eV to $E_i + 0.3$ eV observed at the F/O interface for the 1150°C annealed samples is not clearly understood. With regard to the possible physical origin of this localized state, it is interesting to compare the results with that of thermal oxide and oxygen-precipitated silicon [67]. One possible source is dislocation loop generated around the F/O interface and the other is a trivalent silicon dangling bond state, the so-called P_b center. As far as the dislocation-related states are concerned, it is known that dislocations in silicon exhibit a band of energy states around $E_i + 0.18$ eV [68]. On the other hand, it has been reported [69,70] that the P_b center has an amphoteric nature with an acceptor state at $E_i + 0.31$ eV. These energy levels are very similar to that of the localized state observed in the 1150°C annealed samples. The energy difference may be attributed to the assumed value of electron capture cross section chosen to determine the energy levels shown

in Fig. 4.14. It is noted that precipitates, dislocations, and P_b centers have been reported in SIMOX substrates by cross-sectional transmission electron microscopy (TEM) and electron spin resonance (ESR), respectively [3,37,71]. It is shown that a 1150°C anneal restored the crystallinity of the silicon film with a high density of oxygen precipitates. For SIMOX substrates with the same oxygen dose, a 1250°C anneal for 2 hrs was sufficient to dissolve oxygen precipitates in the silicon film and to out-diffuse excess oxygen. Reduction of oxygen precipitates, dislocations, and P_b centers in the SIMOX substrates annealed at high temperature (> 1250°C) has been ascribed to oxygen out-diffusion and/or oxygen migration towards the buried oxide interfaces [3,37,71]. This result is consistent with our DLTS measurements in which the densities of interface traps as well as localized states are smaller for the 1250°C annealed samples than for the 1150°C annealed samples.

4.4 Conclusion

In this Chapter we have employed three different transient capacitance techniques, well known for MOS capacitors, to determine the generation lifetimes and interface trap profiles at the F/O and S/O interfaces of the SIMOX SIS capacitors. By scanning the quiescent bias voltage and keeping the rate window or temperature fixed, we are able to perform trap filling measurements which can easily distinguish the interface states from the bulk traps. Minority carrier generation process can also be suppressed by lowing the measurement temperature or keeping the Fermi level above midgap. By taking the charge coupling between the F/O and S/O interfaces into account, we have extended the bias-scan DLTS technique to a SIMOX SIS capacitor. Reasonable agreement was obtained for the SIMOX SIS capacitors from both the conductance and the bias-scan DLTS measurements.

We have also demonstrated that the conventional Zerbst and temperature-scan DLTS measurements can be used to study τ_g and D_{it} in the SIS capacitors at both the film and the substrate. This is made possible by pulsing a SIS capacitor into deep

depletion in order to eliminate the charge coupling at the film and the substrate, and to separate the fast transient signals at one interface from the slow carrier emission transients at the other interface. For SIMOX samples studied here, we have observed a longer τ_g and a smaller D_{it} at higher anneal temperature. This improvement may be related to the annealing out of precipitates, dislocations, and silicon dangling bond states near the buried oxide interface of the SIMOX wafers.

Table 4.1 Summary of C-V, C-t, and temperature-scan DLTS analysis on SIS capacitors formed by oxygen implantation. t_{ox}: buried oxide thickness, N_d: doping concentration, τ_g: generation lifetime, and D_{it}: midgap interface state density. The numbers 1 and 2 refer to the film and the substrate, respectively.

Parameter	1150°C, 3 hrs Anneal	1250°C, 2hrs Anneal
t_{ox} (μm)	0.30	0.34
N_{d1} ($\times 10^{15}$ cm^{-3})	19	3.4
N_{d2} ($\times 10^{15}$ cm^{-3})	2.8	2.6
τ_{g1} (μs)	0.0023	0.18
τ_{g2} (μs)	4.5	4.9
D_{it1} ($\times 10^{10}$ cm^{-2}eV^{-1})	21	2.2
D_{it2} ($\times 10^{10}$ cm^{-2}eV^{-1})	3.1	1.5

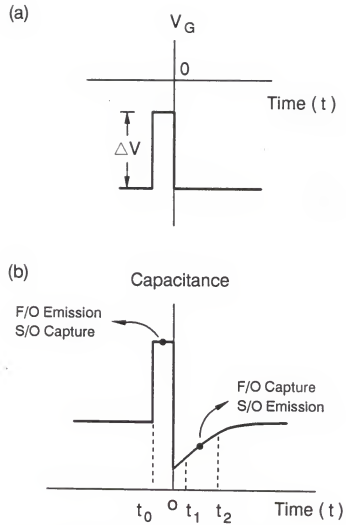

Figure 4.1 Sequence of the bias voltage (a), resulting capacitance transient (b), and energy band bending and electron occupancy of interface states at the film/oxide and the substrate/oxide interfaces (c) of a SIS capacitor.

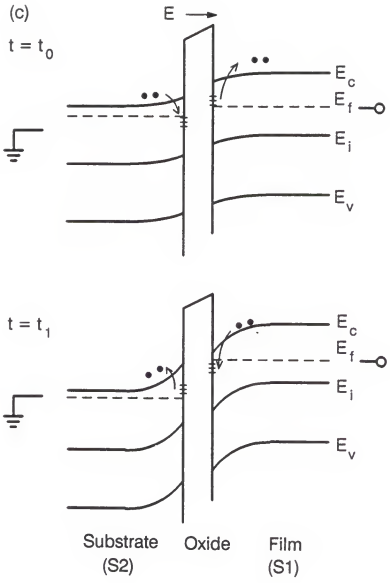

Figure 4.1 – Continued

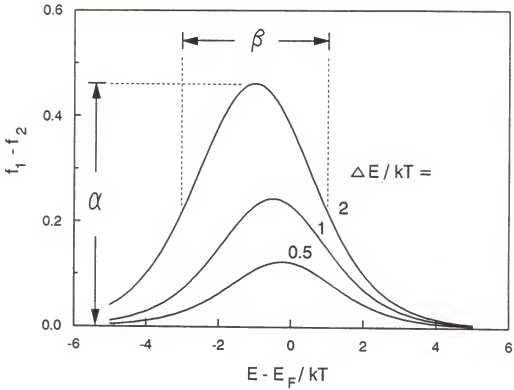

Figure 4.2 The function $(f_1 - f_2)$ versus energy $(E - E_F)/kT$. The parameter $\Delta E/kT$ is related to the trap filling pulse ΔV; α denotes the height and β is the full width at half maximum.

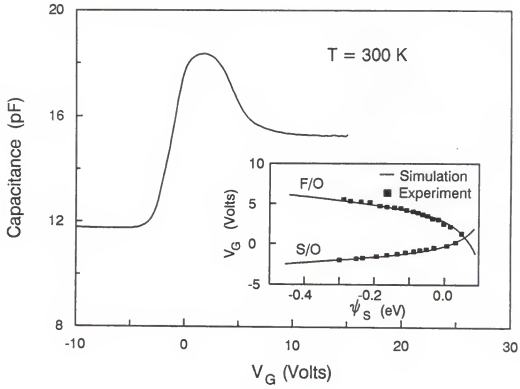

Figure 4.3 High-frequency C-V curves measured at room temperature. Inset shows the gate bias versus surface potential determined by using modified Terman's method.

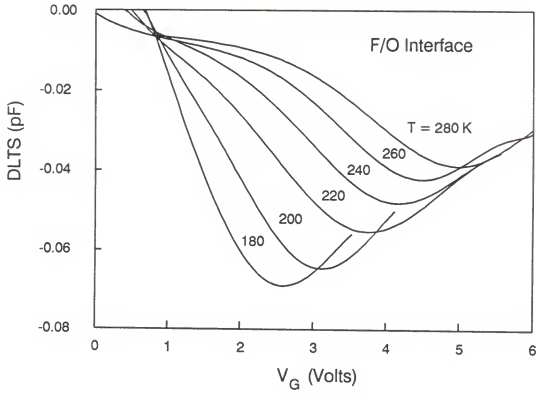

Figure 4.4 Bias-scan DLTS of the film/oxide interface for different temperatures at rate window $t_2/t_1 = 100/20$ μs.

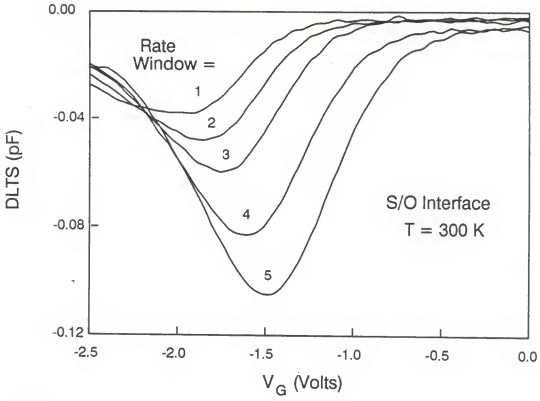

Figure 4.5 Bias-scan DLTS of the substrate/oxide interface at 300 K for different rate windows t_2/t_1 = (1) 1000/200 (2) 500/100 (3) 250/50 (4) 100/20 (5) 50/10 μs.

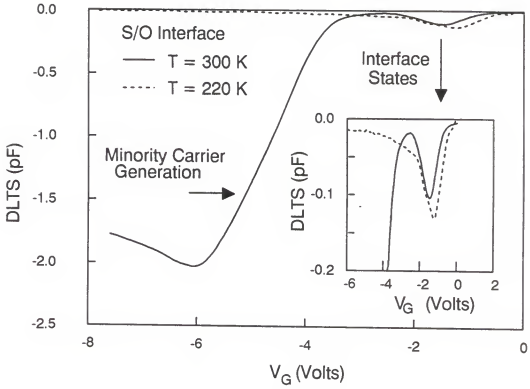

Figure 4.6 Bias-scan DLTS performed at different temperatures showing the temperature dependency of the minority carrier generation.

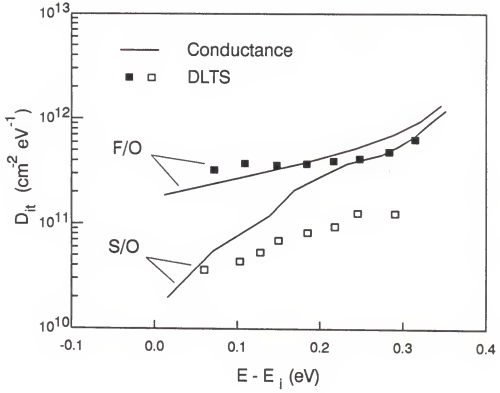

Figure 4.7 Interface state density distribution determined by the conductance (lines) and the bias scan DLTS (squares) measurements at the film/oxide and the substrate/oxide interfaces.

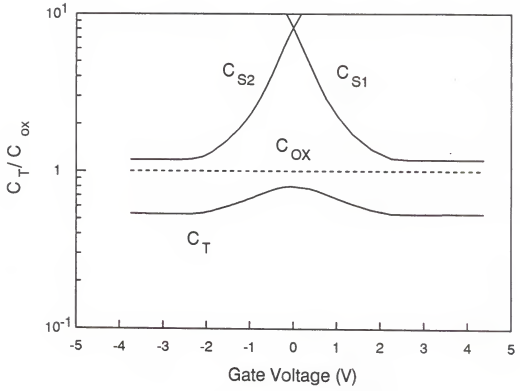

Figure 4.8 Surface capacitance (C_{s1}, C_{s2}), buried oxide capacitance (C_{ox}), and total capacitance (C_T) of a SIS capacitor versus gate voltage. $N_{d1} = N_{d2} = 10^{15}$ cm^{-3} and $t_{ox} = 350$ nm. Interface state density and fixed oxide charge density are assumed equal to zero at the F/O and the S/O interfaces.

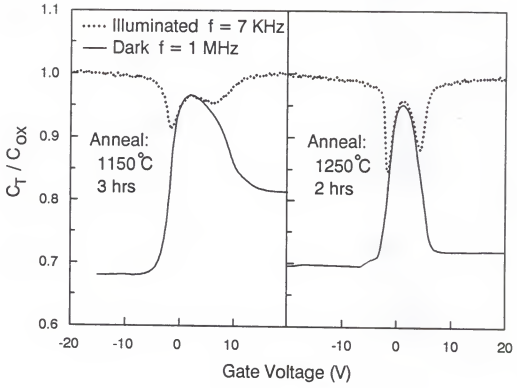

Figure 4.9 Quasi-static capacitance (under illumination) and high-frequency capacitance (in the dark) of the SIS capacitors receiving different post implantation annealing. The small signal frequencies are 7 kHz and 1 MHz for quasi-static and high-frequency capacitance measurements, respectively.

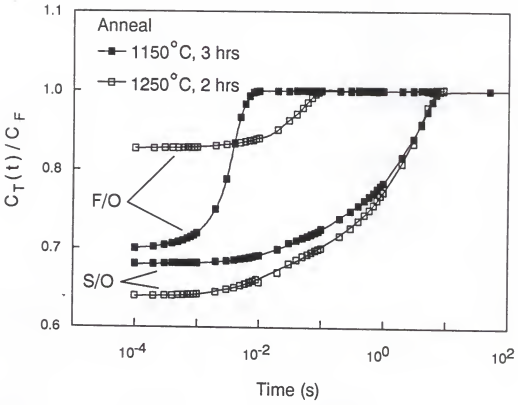

Figure 4.10 Typical C-t responses of the SIS capacitors receiving different post implantation annealing. The measurements are made by pulsing either the film or the substrate into deep depletion.

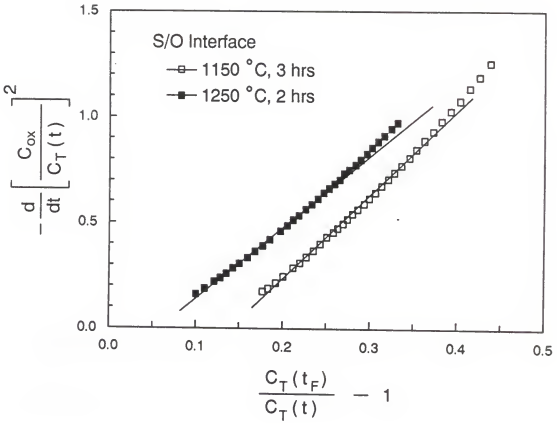

Figure 4.11 Zerbst plot of the SIS capacitors receiving different post implantation annealing at the substrate.

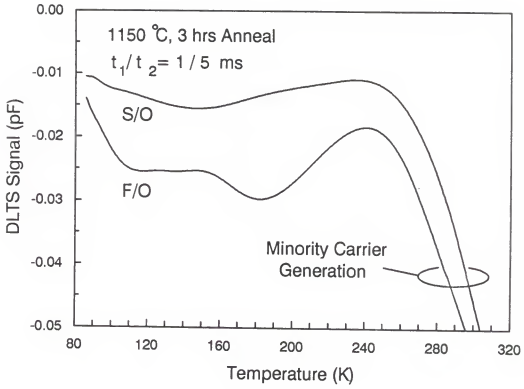

Figure 4.12 DLTS spectra for the SIS capacitors annealed at 1150 °C for 3 hours.

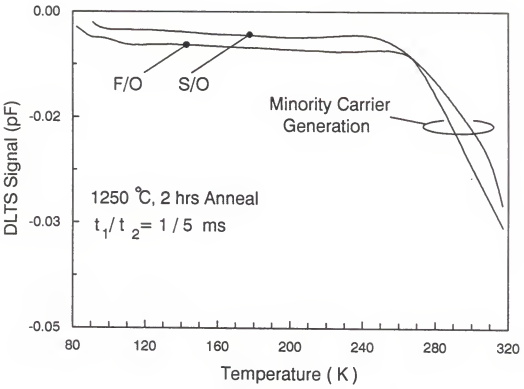

Figure 4.13 DLTS spectra for the SIS capacitors annealed at 1250 °C for 2 hours.

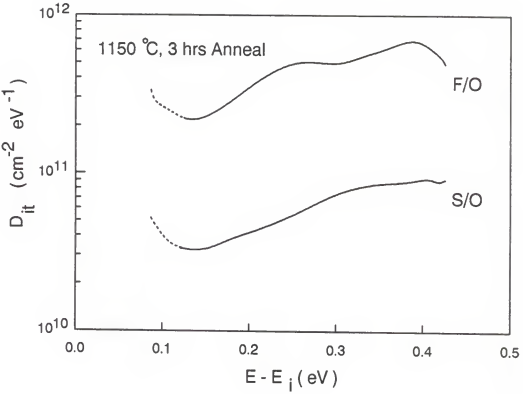

Figure 4.14 Interface state profile obtained from the DLTS analysis of Fig. 4.12, assuming a constant capture cross section of 10^{-15} cm^2.

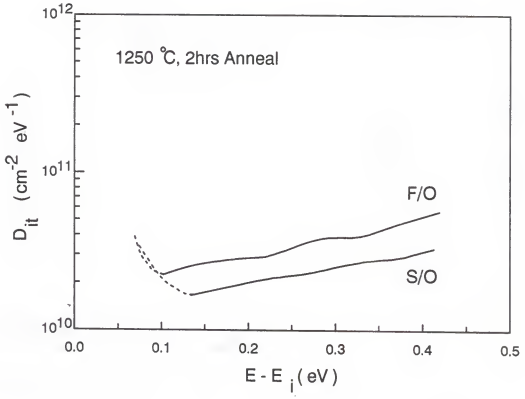

Figure 4.15 Interface state profile obtained from the DLTS analysis of Fig. 4.13, assuming a constant capture cross section of 10^{-15} cm^2.

CHAPTER 5
INTERFACE STATE CHARACTERIZATION IN SMALL GEOMETRY MOSFET'S

5.1 Introduction

Characterization of interface states in small geometry MOSFET's is a subject of intensive research in recent years. Due to the very small gate area of VLSI MOSFET's, conventional capacitance and conductance methods are not possible for characterization of interface states. Deep-level transient spectroscopy [55,72] and charge pumping technique [73,74] are capable of producing quantitative information on the interface properties as well as their capture cross sections. However, these techniques require variation of temperature in order to obtain complete information on interface state properties.

Transconductance is one of the most important parameters for the characterization of a MOSFET, since it is sensitive to the interface states and fixed oxide charges, and is frequently used to monitor the effect of hot-carrier stress and accelerated aging on device reliability [75,76,77]. Recently, several analytical models have been developed, which provide a direct correlation between the dynamic transconductance and the interface state admittance in the depletion- and enhancement-mode MOSFET's [42,78]. Based on these models, it is shown that the interface state density can be determined from the measurement of the imaginary part of the transconductance. However, the real part of the transconductance and the interface state energy profile have been neglected in their work.

In this chapter, we employ the real part of the transconductance to extract the interface state density in a small geometry MOSFET. The real part of the transconduc-

tance can provide identical information as that of the imaginary part of the transconductance. Furthermore, the energy distribution of the interface state density can only be determined from the real part of the transconductance or the static drain current. In fact, the idea is very interesting since it implies that the small signal transistor current can furnish the same information about the interface states as the small signal capacitor current which is several orders of magnitude lower due to the very small gate area.

5.2 MOSFET Equivalent Circuits

Figure 5.1 shows the equivalent circuit of an n-MOSFET with the source and drain tied together (the source and drain are short circuited from the point of view of a.c. signal since there is no load on the drain side). Interface states are represented by the capacitance C_{it} whereas the resistance R_{nt} and R_{pt} account for the energy loss during electron and hole transfer between interface states on one side and the conduction and valence bands on the other side. In weak inversion, interface states are, primarily, in communication with the minority carrier band (conduction band in our case) so that the interface state time constant τ_{it} is equal to $R_{nt}C_{it}$. According to [46], τ_{it} is given by:

$$\tau_{it} = \frac{f}{\sigma_n n_s v_{th}} \tag{5.1}$$

where f is the Fermi function, σ_n is the electron capture cross section, n_s is the surface electron concentration, and v_{th} is the thermal velocity. For a transistor of channel doping $N_a = 10^{16}$ cm^{-3} and a cross section of value $\sigma_n = 10^{-16}$ cm^2, τ_{it} varies between 0.1 and 10^{-7}s as the surface potential ψ_s changes from ϕ_B to $2\phi_B$ (ϕ_B being the difference between the bulk Fermi level and the intrinsic one).

The depletion layer is simply represented by a capacitance C_d due to the very small relaxation times associated with majority carriers which can rest in dynamic equilibrium with the applied signal up to very high frequencies. On the other hand,

the inversion layer resistance R_i limits the rapidity of the inversion layer formation from minority carriers supplied by the drain and source. The problem of the inversion layer formation delay can be treated by using a transmission line model as in [79]. Neglecting the effect of the interface states, the channel time constant τ_{gc} is given by [79]:

$$\tau_{gc} = \frac{C r_i L^2}{4} \tag{5.2}$$

where $r_i = 1/(\mu_{eff} Q_i)$ is the sheet resistance of the inversion layer of absolute charge Q_i and effective mobility μ_{eff}, L is the effective channel length and C is a capacitance given by [79]

$$C = \frac{C_i(C_{ox} + C_d)}{C_{ox} + C_d + C_i} = \frac{C_{ox} + C_d}{C_{ox}} C_{gc} \tag{5.3}$$

where C_{ox} is the gate oxide capacitance, C_i the inversion charge capacitance ($C_i = dQ_i/d\psi_s$) and with $C_{gc} = dQ_i/dV_g$, V_g being the gate voltage. Based on (5.2), theoretical plot of τ_{gc} as a function of V_g for a MOSFET, with a substrate doping of 5×10^{16} cm^{-3} and an oxide thickness of 32.5 nm, is shown in Fig. 5.2 with channel length as a parameter.

It is easily seen that τ_{gc} is essentially constant in weak inversion and decreases with increasing V_g in strong inversion. This result is not surprising since in weak inversion the capacitance C is approximately equal to C_i. Making use of the surface potential dependence of Q_i in weak inversion, the capacitance C_i is given by

$$C_i = \frac{Q_i}{kT/q} \tag{5.4}$$

Consequently, the product $C_i r_i$ is constant and τ_{gc} is given by [78]:

$$\tau_{gc} = \frac{L^2}{4\mu_{eff} Q_i} \frac{(C_{ox} + C_d)C_i}{C_{ox} + C_d + C_i} \tag{5.5}$$

Making use of (5.4) and bearing in mind that, in weak inversion, $C_i \ll (C_{ox} + C_d)$ and $\mu_{eff} \approx \mu_o$, we obtain [78]

$$\tau_{gc} \sim \frac{L^2}{4\mu_o(kT/q)} \tag{5.6}$$

On the other hand, in strong inversion, the capacitance C is approximately equal to C_{ox} and τ_{gc} can, therefore, be expressed as [78]:

$$\begin{aligned} \tau_{gc} &\simeq \frac{C_{ox}L^2}{4\mu_{eff}Q_i} \\ &= \frac{L^2}{4\mu_{eff}(V_g - V_{th})} \end{aligned} \tag{5.7}$$

where $\mu_{eff} = \mu_o/[1 + \theta(V_g - V_{th})]$, V_{th} is the threshold voltage, and θ is the mobility reduction factor. (5.7) indicates that τ_{gc} decreases with increasing V_g due to the rapid increase of Q_i and becomes saturated at relatively high V_g values due to μ_{eff} reduction.

Figure 5.3 shows a theoretical plot of channel time constant versus effective channel length in weak inversion ($\psi_s = \phi_B$). It is obvious from the above arguments that, for transistors of channel lengths less than 10 μm operating in the weak inversion regime, the channel time constant τ_{gc} is much smaller than the minimum value of τ_{it} in weak inversion. Consequently, one can neglect the phase shift due the lateral transport of inversion carriers up to frequencies much higher than that at which the interface states become totally inactive. Therefore, the inversion layer may be simply represented by the capacitance C_i and a transmission line model is not necessary. On the other hand, for channel lengths greater than 10 μm, τ_{gc} becomes comparable to τ_{it}. In this case, not only a transmission line representation of the inversion layer is necessary but also the effect of interface states on the channel time constant τ_{gc} has to be considered.

5.3 Static and Dynamic Transconductance of MOSFET's

In contrast to the MOS capacitor theory, the imaginary part of g_m is similar to the conductance and the real part of g_m is similar to the capacitance. The real part of g_m provides a simple method for interface state characterization across a wide range of forbidden bandgap. However, the imaginary part of g_m is a more accurate, but a more

time consuming technique. The real part of g_m can provide the same information as that of the imaginary part of g_m. Furthermore, the energy distribution of the interface states can only be obtained from the real part of g_m.

We consider an n-channel MOSFET with a gate length smaller than 10 μm. When the transistor is in the ohmic region of operation, the drain current-voltage $I_d(V_d)$ characteristics can be expressed by

$$I_d = \frac{W}{L}\mu_{eff}Q_iV_d \tag{5.8}$$

where W and L are the channel width and length, μ_{eff} is the effective mobility, Q_i is the absolute inversion layer charge, and V_d is the drain voltage. In weak inversion, (5.8) is valid for $V_d < 4kT/q$. The transconductance $g_m = dI_d/dV_g$ is, therefore, given by [78]

$$g_m = \frac{WC_{ox}V_d}{L}\frac{\mu_{eff}^2}{\mu_o}\frac{C_i}{C_{ox}+C_d+C_i+Y_{it}/j\omega} \tag{5.9}$$

where $Y_{it} = G_p + j\omega C_p$ is the interface state admittance.

In weak inversion, the effective mobility takes a constant value μ_o when neglecting surface potential fluctuations and that the inversion charge capacitance C_i is equal to $Q_i/(kT/q)$ so that $g_m(\omega)$ becomes:

$$g_m = \frac{I_d}{(kT/q)}\frac{C_{ox}}{C_{ox}+C_d+C_i+Y_{it}/j\omega} \tag{5.10}$$

It is worth noting that, for $\omega \sim 0$, $Y_{it} = j\omega C_{it}$ (C_{it} is the interface state capacitance). Thus, (5.10) can be expressed as

$$\mathrm{Re}\left\{g_m^{LF}\right\} = \frac{I_d}{(kT/q)}\frac{C_{ox}}{C_{ox}+C_d+C_i+C_{it}} \tag{5.11}$$

In the case of high-frequency ($\sim$ 1 MHz) operation, the frequency is high enough that the interface traps cannot follow the a.c. signal, yet the phase shift due to the lateral transport of inversion carriers is negligible. Therefore, $C_{it} = 0$ and (5.10) reduces to the high-frequency transconductance expression:

$$\mathrm{Re}\left\{g_m^{HF}\right\} = \frac{I_d}{(kT/q)}\frac{C_{ox}}{C_{ox}+C_d+C_i} \tag{5.12}$$

Figure 5.4 illustrates the simulated high- and low-frequency transconductance curves versus V_g with interface state density as a parameter. The model in [80] has been used for the calculations, but the expressions in [81] or [82] provide practically identical curves. It is noted that as the interface state density increases, the difference between the high- and low-frequency transconductance curves increases, and the maximum of the low-frequency transconductance curve decreases. The mobility degradation due to the increased interface state density is not taken into account in this calculation. Therefore, the maximum high-frequency transconductance remains constant as the interface state density increases.

5.4 Extraction of Interface Properties from the Transconductance

The high-frequency, low-frequency, and combined high-low frequency transconductance methods use the real part of g_m, and the dynamic transconductance method uses the imaginary part of g_m for evaluation of the interface state properties in a small geometry MOSFET. These methods are described as follows:

5.4.1 High-Frequency Transconductance Method

In the high-frequency transconductance method, transconductance is measured as a function of gate bias with frequency fixed at a high enough value so that interface traps do not response. For a MOSFET with gate length smaller than 10 μm, interface traps do not follow the ac gate voltage in a high frequency $g_m - V_g$ measurement, but they do follow very slow changes in gate bias as the MOSFET is swept from depletion to inversion. Since interface traps do not respond to the ac gate voltage, they contribute no effect to the high frequency $g_m - V_g$ curve. However, as interface traps follow the changes in gate bias, they cause the high frequency $g_m - V_g$ curve to stretch out along the gate bias axis. Therefore, measuring the high-frequency transconductance g_m^{HF} in a MOSFET will be the same as that of an ideal one without interface traps if the band bending is the same. Knowing ψ_s corresponding to the

same g_m^{HF} in an ideal MOSFET and measuring V_g corresponding to the same g_m^{HF} in a real MOSFET, we can construct a ψ_s versus V_g for the MOSFET with interface traps.

By graphical or numerical differentiation of the ψ_s versus V_g curve, the derivative $d\psi_s/dV_g$ is found. In analogy to the high-frequency capacitance method, $C_{it}(\psi_s)$ can be expressed by

$$C_{it} = C_{ox}\left[\left(\frac{d\psi_s}{dV_g}\right)^{-1} - \frac{I_d}{(kT/q)}\mathrm{Re}\left\{\frac{1}{g_m^{HF}}\right\}\right] \tag{5.13}$$

Therefore, if C_{it} is found from (5.13), then D_{it} can be calculated by using $C_{it} = qD_{it}$.

5.4.2 Low-Frequency Transconductance Method

The low-frequency $g_m - V_g$ method is similar to that of the low-frequency capacitance method developed by Berglund [51]. Again, $g_m - V_g$ curve is measured at a constant frequency, but at a frequency so low that the interface traps immediately respond to the ac gate voltage, they will contribute an additional component to the measured low frequency or static $g_m - V_g$ curve. In addition, interface traps follow changes in gate bias so that the measured low-frequency transconductance curve will be stretch out along the gate bias axis like the high-frequency $g_m - V_g$ curve. Solving (5.11) for C_{it} yields

$$C_{it} = \frac{I_d C_{ox}}{(kT/q)}\mathrm{Re}\left\{\frac{1}{g_m^{LF}} - \frac{1}{g_{ms}}\right\} \tag{5.14}$$

where g_{ms} is the ideal transconductance. The value of $g_{ms}(V_g)$ is obtained by calculation. There are two steps in this calculation. First, g_{ms} is calculated as a function of ψ_s. Second, g_m^{LF} can be related to g_{ms} if ψ_s versus V_g is known.

Surface potential versus gate voltage can also be obtained experimentally from the low-frequency $g_m - V_g$ curve alone. First, $d\psi_s/dV_g$ is obtained by differentiating the charge conservation relation with respect to surface potential ψ_s:

$$\frac{d\psi_s}{dV_g} = \frac{C_{ox}}{C_{ox} + C_d + C_i + C_{it}} \tag{5.15}$$

From (5.11) and (5.15) we obtain

$$\frac{d\psi_s}{dV_g} = \frac{(kT/q)}{I_d} Re\left\{g_m^{LF}\right\} \tag{5.16}$$

Integrating from the threshold voltage V_{th} to V_g, (5.16) becomes

$$\psi_s(V_g) \simeq V_d + 2\phi_B + \frac{kT}{q}\int_{V_{th}}^{V_g} Re\left\{\frac{g_m^{LF}}{I_d}\right\} dV_g \tag{5.17}$$

The integrand in (5.17) is determined from measured g_m^{LF} and I_d versus V_g curves. Since $g_m^{LF} = dI_d/dV_g$, (5.17) can be expressed in terms of I_d as

$$\psi_s(V_g) \simeq V_d + 2\phi_B + \frac{kT}{q}\ln\left[\frac{I_d(V_g)}{I_d(V_{th})}\right] \tag{5.18}$$

By measuring I_d and V_{th}, the relationship between ψ_s and V_g can be easily established.

5.4.3 High-Low Frequency Transconductance Method

The method discussed in this section is similar to that of the combined high-low frequency capacitance method [49]. The combined high-low frequency transconductance method eliminated the need for a theoretical computation of g_{ms} and for measurement of the doping profile of the device. Using (5.11) and(5.12), C_{it} can be expressed in terms of measured g_m^{LF} and g_m^{HF} as

$$C_{it} = \frac{I_d C_{ox}}{(kT/q)} Re\left\{\frac{1}{g_m^{LF}} - \frac{1}{g_m^{HF}}\right\} \tag{5.19}$$

In this way C_{it} is obtained directly from the measured $g_m - V_g$ curves without the uncertainty introduced by a theoretical calculation of g_{ms} and without uncertainty as to whether g_{ms} has been calculated for the correct band bending. Note that (5.19) yields C_{it} only as a function of gate bias. Interface state density is obtained as a function of energy by using the low-frequency or high-frequency transconductance method. It is noted that the only device parameter required to calculate the interface state density is oxide thickness which can be determined with good accuracy. Therefore, the uncertainty in determining the mobility, gate length, and channel doping profile of a MOSFET can be eliminated.

5.4.4 Dynamic Transconductance Method [78]

In analogy to the MOS conductance method, dynamic transconductance method can be applied to a MOSFET for interface state characterization. In particular, the imaginary part of $1/g_m$ can be related to the interface state parallel conductance G_p by [78]:

$$\frac{G_p}{\omega} = \frac{C_{ox} I_d}{(kT/q)} \mathrm{Im}\left[\frac{1}{g_m(\omega)}\right] \tag{5.20}$$

Subsequently, G_p/ω can be deduced from combined measurements of dynamic transconductance and drain current. In the case of an interface state continuum and in absence of surface potential fluctuations, G_p/ω is related to the interface state density D_{it} by the following expressions [46]

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln(1 + \omega^2 \tau_{it}^2) \tag{5.21}$$

where τ_{it} is the interface state time constant.

5.5 Results and Discussion

Transconductance measurements have been made on conventional n-channel MOSFET's with channel length of 2.5 μm and width of 50 μm. The doping density under gate oxide (32.5 nm) is about 5×10^{16} cm^{-3}. Transconductance measurements were performed at frequencies of 1 MHz and 10 Hz using a HP 4192A impedance analyzer with drain voltage kept at 30 mV during all measurements. The electrical circuit of the experimental setup is schematically represented in Fig. 5.5.

In order to test our method, we have performed transconductance measurements on the bulk MOSFET's which were degraded by high field (Fowler-Nordheim) injection. Such an electrical stress is well known to create interface states uniformly distributed along the channel. In our case, the gate electrode of the MOSFET's was biased at 20 V for 20 min with drain and source floating. The results of the transconductance versus gate bias measurements before and after high field stress are shown

in Fig. 5.6. As can be seen in this figure that the difference between the high- and the low-frequency transconductance increases after high field stress which implies an increase in the interface state density. The inset in Fig. 5.6 shows a typical double-plateau dependence of the real part of g_m on frequency for a pre-stressed MOSFET biased in weak inversion. This behaviour has been previously reported by Becke et al. [83]. The variation of the real part of g_m with frequency is related to the frequency dependent C_{it}, since C_{ox}, C_d, and C_i are frequency independent.

Figure 5.7 shows the distribution of interface traps in the bandgap determined from (5.18) and (5.19) and for a MOSFET before and after high field stress. The inset in Fig. 5.7 shows the corresponding ψ_s versus V_g curves determined by using (5.18). Such a determination is valid only in a limited energy range of the forbidden gap. This range extends from the beginning of weak inversion (in our case, limited by the sensitivity of impedance analyzer) to the onset of strong inversion ($V_g = V_{th}$). Changes in transistor transconductance ($\Delta g_m/g_m$), threshold voltage (ΔV_{th}) and charge pumping current (ΔI_{cp}) have been widely used as a measure of degradation [75] - [77]. The three measures of degradation and the interface state densities determined by the high-low frequency transconductance method, normalized to their maximal values, are plotted as a function of stress time in Fig. 5.8. Reasonable agreement was obtained between these methods.

We also applied high-low frequency transconductance method to partially-depleted thin-film (0.5 μm) SOI MOSFETs. Two types of samples are used in this study. One is prepared by single oxygen implant to a dose of 1.5×10^{18} cm^{-2} followed by annealing at 1285°C for 2 h. The other is prepared by multiple oxygen implants to a total dose of $4 \times (4 \times 10^{17})$ cm^{-2}, where each 4×10^{17} cm^{-2} implantation was followed by annealing at 1285°C for 2 h. The multiple implantation is known to produce SIMOX substrates of very high quality [84]. Figure 5.9 shows the measured high- and low-frequency transconductance curves of the single- and multiple-implanted MOSFETs,

respectively. The distribution of interface traps determined by the high-low frequency transconductance method is shown in Fig. 5.10 for both types of samples. As expected, the interface state density of the multiple-implanted samples is very small compared to that of the single-implanted samples. The low interface state density found in multiple-implant SIMOX confirms the promises of this technology.

5.6 Conclusion

In conclusion, we have demonstrated, for the first time, that the real part of the transconductance can be applied to assess the interface properties in small geometry MOSFET's. Moreover, we relate the surface potential versus gate bias by using the static drain current measurement, which enables us to obtain the interface state profile. Finally, the method presented here can be very useful for the characterization of hot carrier stress and silicon-on-insulator structures.

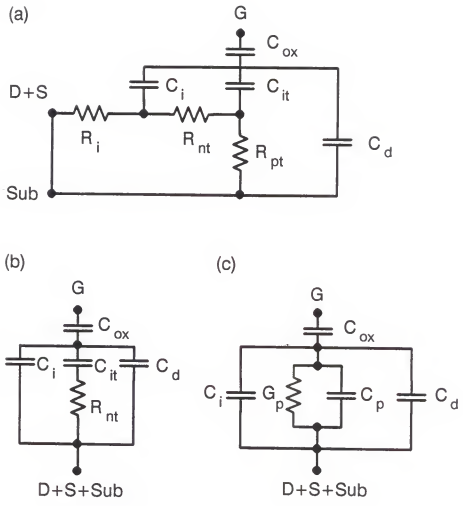

Figure 5.1 Equivalent circuit of a MOSFET with the drain and source tied together and connected to the substrate. The three different figures correspond to (a) general case where the resistance R_i accounts for the inversion layer formation delay, (b) case of a relatively short channel device ($L < 10\ \mu m$) operating in inversion, and (c) same case as (b) but the interface state series impedance has been replaced by its equivalent parallel admittance [78].

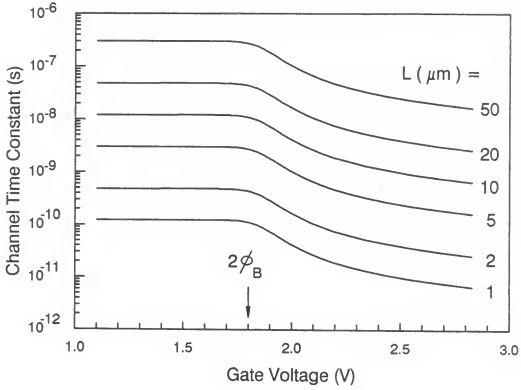

Figure 5.2 Theoretical channel time constant versus gate voltage calculated for MOSFET's of different channel lengths (from 1 to 50 μm) and having $N_a = 5 \times 10^{16}$ cm^{-3}, $T_{ox} = 32.5$ nm, and $\mu_o = 800$ cm^2/Vs (without interface traps and fixed oxide charge).

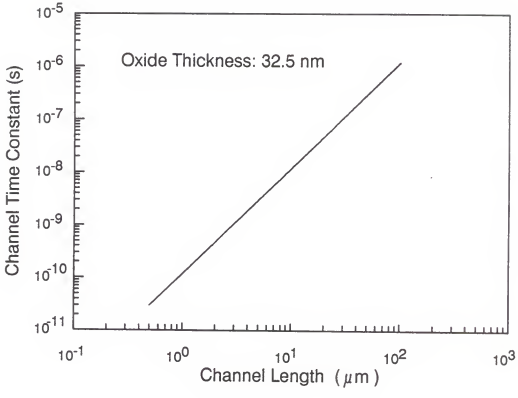

Figure 5.3 Theoretical channel time constant versus channel length and having $N_a = 5 \times 10^{16}$ cm^{-3}, $T_{ox} = 32.5$ nm, and $\mu_o = 800$ cm^2/Vs (without interface traps and fixed oxide charge).

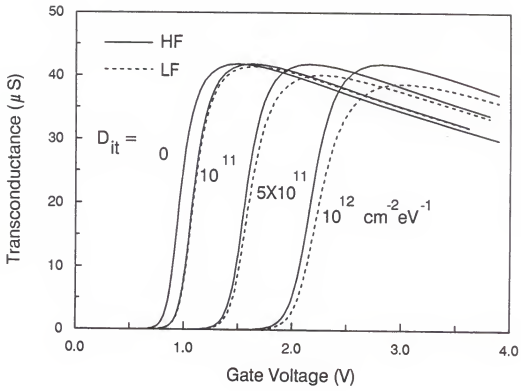

Figure 5.4 Simulated high- and low- frequency transconductance curves versus V_g with interface state density as a parameter. L = 2.5 μm, W = 50 μm, $N_a = 5 \times 10^{16}$ cm^{-3}, and T_{ox} = 32.5 nm.

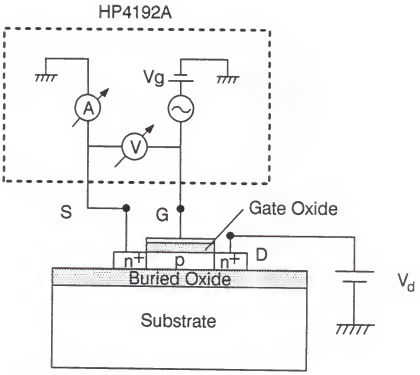

Figure 5.5 Schematic diagram of the experimental setup used for the MOSFET transconductance measurements [78].

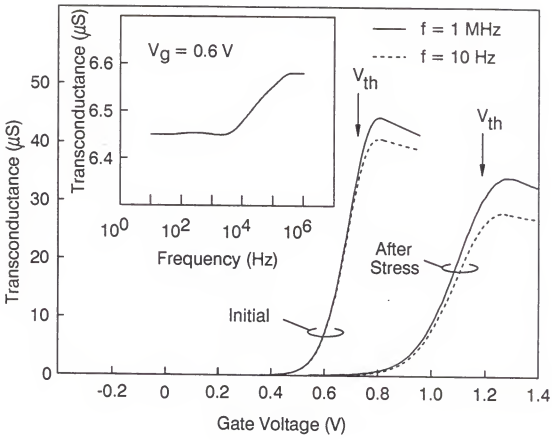

Figure 5.6 Typical high- and low- frequency transconductance versus gate bias of a bulk MOSFET before and after Fowler-Nordheim injection. The variation of the real part of the transconductance with frequency in weak inversion is shown in the insertion.

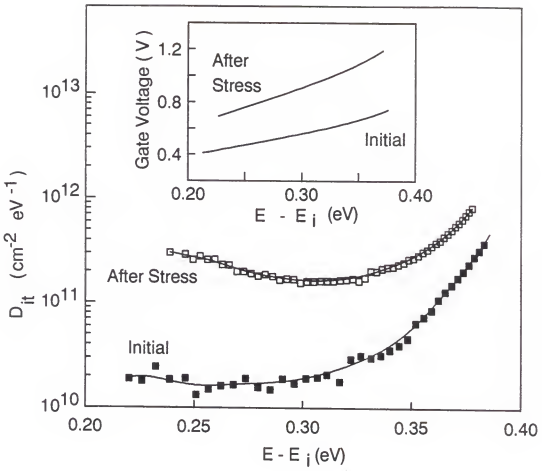

Figure 5.7 Interface state density D_{it} versus energy (relative to midgap) of a bulk MOSFET before and after Fowler-Nordheim injection. The inset shows the corresponding surface potential (expressed in terms of $E - E_i$, where E_i is the intrinsic Fermi energy) versus gate bias.

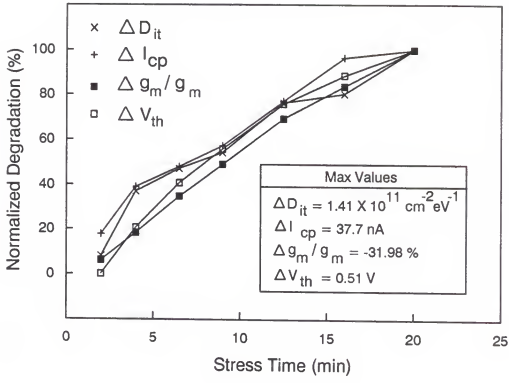

Figure 5.8 Normalized degradation determined by changes in transistor transconductance ($\Delta g_m/g_m$), threshold voltage (ΔV_{th}), charge pumping current (ΔI_{cp}), and high-low frequency transconductance method (ΔD_{it}) versus stress time.

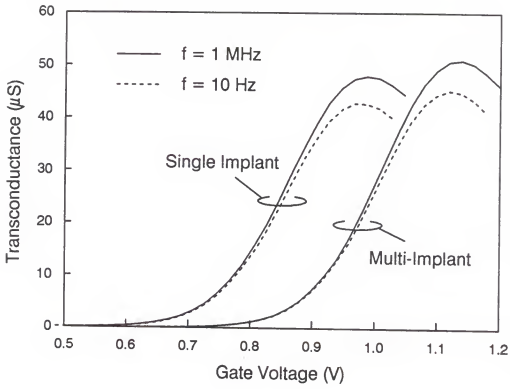

Figure 5.9 The measured high- and low- frequency transconductance curves for single- and multiple- implanted SOI MOSFETs, respectively. Both samples have a partially-depleted film of 0.5 μm. The transconductance curves of the multi-implanted sample are shifted horizontally for clarity.

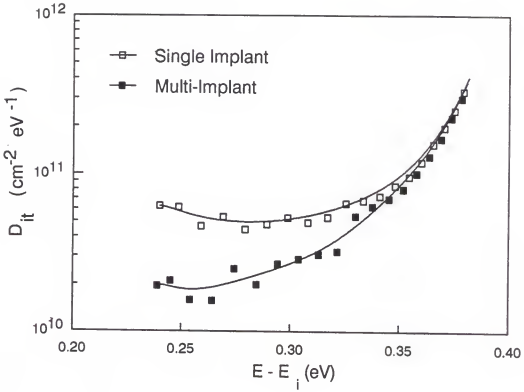

Figure 5.10 The distribution of interface traps determined by the high-low frequency transconductance method for both single- and multiple- implanted SOI MOSFETs.

CHAPTER 6
DESIGN CONSIDERATIONS FOR YIELD ENHANCEMENT OF SOI MOSFET'S

6.1 Introduction

The demand for more complex MOS VLSI circuits has continued to push for scaling down in device geometries. The production of these VLSI circuits requires an aggressive scaling of device geometries, in order to achieve the desired circuit functions and speed. The scaling of feature size has progressed more rapidly than the scaling of process tolerance. As a result, at the micrometer and submicrometer geometries used in the current VLSI circuit design, these device parameters are no longer deterministic, but behave rather as probabilistic random variables with a certain probability distribution. These random fluctuations in IC fabrication processes are becoming the predominant factor in causing the production yield to fall below acceptable levels. They determine not only circuit nominal performance but also "ease of fabrication," or simply manufacturability of the developed product. Therefore, a high level of manufacturability of an IC can be seen as an extra design goal, and it is as important as the IC performance itself [85].

Thin film SOI technology is potentially advantageous for VLSI circuits because of the unique benefits offered by SOI MOSFET's. Previous work has demonstrated that the thin-film SOI MOSFET does have advantage over the bulk MOSFET, including reduced hot-carrier effects [86,87], enhanced current drive [88], attenuated short-channel effects [89,90], and reduced temperature dependence of threshold voltage [91]. However, current SIMOX technology produces SOI substrates with high density of threading dislocations in the top silicon film [92]. Generation lifetimes

measured in SIMOX wafers are at least one order of magnitude below their bulk silicon counterparts [33]. The interface states in the gate oxide/film and film/buried oxide interfaces are typically greater than 5×10^{10} $cm^{-2}eV^{-1}$ [40,42]. Although, SIMOX material quality is still inferior to bulk silicon material, an increasing body of evidence has shown that yield on the SIMOX based 64K SRAMS is as good as or better than what they would achieve with the same circuit on the bulk silicon material [92].

Using previously developed physical models for the bulk and SOI MOSFETs, we examine in this chapter design considerations to exploit the unique benefits of VLSI circuit manufacturability in thin-film SOI MOSFET. We compare and analyze the statistical variation of the threshold voltage in both the bulk and SOI MOSFETs with respect to variation of device parameters such as doping concentration, oxide thickness, channel length etc. In general, our study reveals that the threshold voltage of fully depleted thin-film SOI MOSFET's is less sensitive to the variation of device parameters, and hence may result in an improved yield over their bulk silicon counterpart.

6.2 Statistical Analysis of Threshold Voltage

Manufacturability of a specific VLSI circuit is determined by many factors involving both the design procedure and the fabrication process. All of these factors, however, have one common characteristic–they cause unacceptable discrepancies between the desired and the actual performance of the fabricated IC. To predict the production yield of an IC may require sophisticated modeling work and extensive numerical simulation. In order to estimate the production yield of VLSI circuits we monitor the statistical distribution of the threshold voltage (a key output parameter) of a MOSFET.

Recently, the statistical variation effect on a short-channel MOSFET has been investigated by assuming that the threshold voltage is a random function of the device

parameters such as channel length L, oxide thickness t_{ox}, substrate doping N_a, and junction depth r_j [93]:

$$V_{th} = V_{th}(L, t_{ox}, N_a, r_j, ...) \tag{6.1}$$

By considering each of the device parameters that can be characterized with a Gaussian distribution, the probability distribution $P(V_{th})$ associated with the threshold voltage, the mean value $\mu(V_{th})$, and the standard deviation $\sigma(V_{th})$ can be calculated.

6.2.1 Threshold Voltage of Bulk MOSFET

The threshold voltage of an n-channel MOSFET is given by [28]

$$V_{th}^{B} = V_{FB} + 2\phi_B + \frac{\sqrt{4q\epsilon_s N_a \phi_B}}{C_{ox}} \tag{6.2}$$

where V_{FB} is the flat band voltage, ϕ_B is the Fermi potential, and C_{ox} is the gate oxide capacitance. The first-order estimation of the short-channel induced threshold voltage reduction in a bulk MOSFET is given by [94]

$$\Delta V_{th}^{B} = \frac{qN_a W_m}{C_{ox}} \frac{r_j}{L} \left[\left(1 + \frac{2W_m}{r_j} \right)^{1/2} - 1 \right] \tag{6.3}$$

where W_m is the maximum depletion layer width, and r_j is the drain/source junction depth.

6.2.2 Threshold Voltage of Thin-Film SOI MOSFET

The threshold voltage of a SOI MOSFET is influenced by the charge coupling between the front and the back gates. For accumulation at the film/buried oxide interface, the threshold voltage is given by [95],

$$V_{th}^{SOI} = V_{FB} + (1 + \alpha)2\phi_B - \frac{Q_b}{2C_{ox}} \tag{6.4}$$

For depletion at the film/buried oxide interface,

$$V_{th}^{SOI} = V_{FB} + 2\phi_B - \frac{Q_b}{2C_{ox}} - \alpha\beta \left(V_{Gb} - V_{FB}^{b} - 2\phi_B + \frac{Q_b}{2C_{ob}} \right) \tag{6.5}$$

where V_{Gb} is the back gate voltage, V_{FB}^{b} is the back gate flat band voltage, t_b is the film thickness, t_{ob} is the back gate oxide thickness, $C_b = \epsilon_s / t_b$ is the depletion

capacitance, $C_{ob} = \epsilon_{ox}/t_{ob}$ is the back gate oxide capacitance, $Q_b = -qN_at_b$ is the depletion-region areal charge, $\alpha = C_b/C_{ox}$, and $\beta = C_{ob}/(C_{ob} + C_b)$. The threshold voltage reduction due to the short channel effect in a SOI MOSFET can be written as [90]

$$\Delta V_{th}^{SOI} = \frac{d}{L}\frac{qN_at_b}{2C_{ox}} \tag{6.6}$$

where d is a factor related to the depletion charge controlled by the front and the back gates.

In the following statistical analysis, the device parameters used in the calculation are summarized in Table 6.1, unless it is specified in each of the figures. We assume a gate material (for both front and back gates) with a work function of intrinsic silicon ($\phi_m = \chi + E_g/2q$), where χ and E_g denote the electron affinity and bandgap energy of silicon, respectively. Various refractory metals such as W, Mo, and the silicides (e.g., WSi_2 and $MoSi_2$) meet this requirement. For p^+ or n^+ polysilicon gates, the work function is determined by adding or subtracting $E_g/2q$ to ϕ_m, respectively. For simplicity, we will assume no fixed oxide charges and interface states at both Si/SiO_2 interfaces, and E_g is independent of temperature over the temperature range under consideration (i.e., 300 – 320 K). For the SOI MOSFET, the back gate voltage is maintained at 0 V.

6.3 Results and Discussion

6.3.1 Variation of Oxide Thickness

Figure 6.1 shows the statistical variation of the threshold voltage $P(V_{th})$ achieved by considering a standard deviation $\sigma(t_{ox})$ of 20 nm in oxide thickness for three different film thicknesses. Other device parameters are considered constant and summarized in Table 6.1. As can be seen, the statistical distribution of a bulk MOSFET is wider than that of a thin-film SOI MOSFET. The probability distribution $P(V_{th}^{SOI})$ for SOI MOSFETs becomes narrower when the film thickness is reduced from 0.3 μm

to 0.1 μm. This conclusion is also verified from the results shown in Fig. 6.2, where, for the same device parameters, the mean value and the standard deviation of the threshold voltage are shown as a function of gate oxide thickness for three different film thicknesses. As expected, the standard deviation of a bulk MOSFET is greater than that of a SOI MOSFET. This result implies a less sensitive threshold voltage variation with respect to the deviation of oxide thickness in a fully depleted SOI MOSFET. Also, reducing the film thickness tends to reduce the standard deviation of the threshold voltage. The reduction of $\sigma(V_{th}^{SOI})$ is expected, since the depletion charge controlled by the gate is smaller in a SOI MOSFET than that of a bulk MOSFET, especially with a thin silicon film. It is noted that although the coefficient of variation (ratio of σ to μ) increases from 5 % to 20 % as the oxide thickness decreases from 40 nm to 10 nm, the standard deviation of the threshold voltage remains constant for both the bulk and SOI MOSFETs. This is due to the decreasing influence of the depletion charge with reducing oxide thickness. This result indicates that scaling the gate oxide thickness has only minor effect on the threshold voltage variation.

6.3.2 Variation of Doping Concentration

Figure 6.3 shows the probability distribution of the threshold voltage with respect to $\sigma(N_a) = 5\times10^{14}$ cm^{-3} for three different doping concentrations in both the bulk and SOI MOSFETs, respectively. It is shown that as the doping concentration decreases the $P(V_{th})$ distribution also widened in both MOSFETs. This is mainly due to the increase of the coefficient of variation $\sigma(N_a)/\mu(N_a)$ as the doping concentration changes from 1.5×10^{16} to 5×10^{15} cm^{-3}. A comparison of the bulk and the SOI MOSFETs with doping concentration of 5×10^{15} cm^{-3} indicates that the broadening effect is less significant in the SOI MOSFET. However, for a SOI MOSFET with doping concentration of 1.0×10^{16} cm^{-3} or higher, the broadening effect becomes more obvious than that of a bulk MOSFET. Figure 6.4 shows the mean value and the standard deviation of the threshold voltage as a function of doping concentration for

three different film thicknesses. The standard deviation $\sigma(V_{th}^{SOI})$ of a SOI MOSFET can be larger or smaller than that of a bulk MOSFET depending on the doping concentration and film thickness.

Optimized design region of a fully-depleted SOI MOSFET with threshold voltage distribution smaller than its bulk silicon counterpart is shown in region I of Fig. 6.5. The solid line is determined from Fig. 6.4 with $\sigma(V_{th}^{SOI}) = \sigma(V_{th}^{B})$. The dashed line is the constrain imposed by the requirement of a fully depleted film. In a conventional MOSFET's, the maximum depletion layer width W_m at the channel region can be described by

$$W_m = \left(\frac{4\epsilon_s\phi_B}{qN_a}\right)^{1/2} \tag{6.7}$$

To achieve full depletion in the SOI film, t_b should be equal to or less than W_m. In region I, the statistical variation of the threshold voltage is less severe in a SOI MOSFET than that of a bulk MOSFET, i.e., $\sigma(V_{th}^{SOI}) < \sigma(V_{th}^{B})$ and in region II, $\sigma(V_{th}^{B})$ is less than $\sigma(V_{th}^{SOI})$. The reduced standard deviation of threshold voltage of a SOI MOSFET (region I), as is compared to that of a bulk MOSFET, is due to the reduced depletion charge controlled by the gate with decreasing film thickness and doping concentration. The increased threshold voltage variation in a SOI MOSFET (region II) can be readily understood by comparing the depletion charge controlled by the gate to that of a bulk MOSFET. In a fully depleted SOI MOSFET, the depletion charge is proportional to N_a (neglect the weak dependence of ϕ_B on N_a). However, in a bulk MOSFET the depletion charge is proportional to $N_a^{1/2}$. Therefore, as the doping concentration increases, the sensitivity of the threshold voltage with respect to doping concentration increases much faster in a SOI MOSFET than that of a bulk MOSFET, which eventually leads to a more severe statistical variation of threshold voltage in a SOI MOSFET. To minimize the variation of the threshold voltage of a SOI MOSFET's, a lightly doped (near intrinsic) channel region with thin silicon film is suggested.

6.3.3 Variation of Channel Length

The threshold voltage reduction due to short channel effect in a SOI MOSFET's is calculated by using (6.6) and assuming of a accumulated film/buried oxide interface. Such an assumption avoids iterations in calculating ΔV_{th}^{SOI} and yet provides insightful information for statistical threshold voltage analysis. Figure 6.6 shows the statistical variation of the threshold voltage, for three values of channel length, achieved by considering a standard deviation $\sigma(L)$ of 0.1 μm in channel length. Other device parameters are assumed constant. As can be seen, the statistical distribution becomes more broadened with a pronounced asymmetry toward the higher value of ΔV_{th}. It is also noted that the statistical distribution in the SOI MOSFET is narrower than that of the bulk MOSFET. This conclusion is also confirmed by the result shown in Fig. 6.7, where, for the same device parameters, the standard deviation of the threshold voltage reduction is shown as a function of channel length. As expected, the standard deviation increases as the channel length decreases, since the effect of $\sigma(L)/\mu(L)$ is much larger for short channel devices. For a SOI MOSFET with accumulated back interface, ΔV_{th}^{SOI} is proportional to t_b/L, as shown in (6.6). Therefore, if the film thickness and the channel length are scaled down, the ΔV_{th}^{SOI} will not vary as much as if t_b were kept constant [90]. Similar argument applies to the standard deviation of ΔV_{th}^{SOI}. As shown in Fig. 6.7, for a given channel length $\sigma(\Delta V_{th}^{SOI})$ decreases as the film thickness decreases.

6.3.4 Variation of Film Thickness

Perhaps the only drawback for a fully depleted SOI MOSFET is the tight control of the film thickness. Variation of the film thickness directly affects threshold voltage. As the film thickness becomes thinner, the acceptable range for variation becomes more stringent. At present the SIMOX technology is capable of producing film uniformity within 10 nm across the wafer [92] which inhibits the use of ultra-thin film SOI MOSFET for VLSI applications. As an example, Fig. 6.8 shows the probability

distributions for three different film thicknesses, calculated by assuming a constant standard deviation $\sigma(t_b)$ of 10 nm. As can be seen, the probability distribution of the threshold voltage becomes more broadened when the film thickness is decreased. Figure 6.9 shows the mean and standard deviation of the threshold voltage as a function of the film thickness. Since the coefficient of variation $\sigma(t_b)/\mu(t_b)$ is higher for thinner film, the standard deviation increases as the film thickness decreases. The effect of nonuniform film thickness on the threshold voltage variation can be eased by using a lower channel doping density or a thinner gate oxide to reduce the influence of depletion charge on the threshold voltage.

6.3.5 Variation of Temperature

Nonuniform temperature distribution across the VLSI chip is expected, since some devices are turned on and some of them are turned off during normal circuit operation. A comparison of the broadening effect in the bulk and the SOI MOSFETs is shown in Fig. 6.10, which is plotted by assuming a standard deviation $\sigma(T)$ of 10 K. A more pronounced broadening effect in the bulk MOSFET is expected since the temperature dependence of the threshold voltage in bulk MOSFET is controlled by both Fermi potential ϕ_B and the maximum depletion width. However, in the case of a fully depleted SOI MOSFET, it is only controlled by ϕ_B. Again, a smaller standard deviation of threshold voltage $\sigma(V_{th}^{SOI})$ can be observed in Fig. 6.11 for the SOI MOSFET.

6.4 Design Considerations

The simulations presented above clearly show a unique advantage of SOI over bulk MOSFET with regard to the threshold voltage sensitivity on statistical variation of device parameters. A properly designed short-channel thin-film SOI MOSFET, with a lightly doped (near-intrinsic) channel region to reduce the sensitivity of threshold voltage on the depletion charge, could enhance the yield of the SOI circuits. The

advantages of near-intrinsic thin-film design are numerous [96] - [98]: (i) increased mobility and subthreshold slope are expected due to the absence of impurity charge; (ii) symmetric threshold voltage for n- and p-channel devices are achieved without channel doping step by using a gate material with the same work function as the intrinsic silicon; (iii) the shallow drain/source junctions are automatically achieved and the spiking problems of a silicide or a metal contact are eliminated by the presence of the buried oxide. However, design tradeoffs involving other device characteristics such as reduced threshold voltage, short-channel effects, and nonuniform film thickness must be considered to ensure the viability of near-intrinsic thin-film MOSFET's.

The near-intrinsic thin-film SOI MOSFET tends to reduce the threshold voltage, but the tradeoff implied can be loosen by using various refractory metal and metal-silicide gates. The short-channel effect, especially punchthrough associated with near-intrinsic channel doping, have been shown not to produce serious constrains on SOI MOSFET's, if the film is made thinner and its channel length is scaled down [90,96,99]. However, the minimum silicon film thickness may be limited by the process technology, the finite channel thickness, or the increased coefficient of variation $\sigma(t_b)/\mu(t_b)$. Present technology is capable of producing a minimum film thickness of about 50 nm [100]. Even though this barrier can be overcome, the problem associated with finite film thickness should be considered. Quantum mechanical calculation indicates an inversion layer thickness of about 10 nm for a normally operated MOSFET [101]. For film thickness under 10 nm, the current drive capability decreases. This is due to the finite film thickness and increased interface roughness scattering at both the front and back gates. With aggressive reduction of film thickness, the effect of nonuniform film thickness may be increased drastically. The increased coefficient of variation $\sigma(t_b)/\mu(t_b)$ as t_b is reduced can be eased by using a thinner gate oxide to reduce the influence of depletion charge on the threshold voltage. It is noted that the penalty (in terms of threshold voltage variation) imposed by the reduction of oxide

thickness is negligible, as was discussed in section III-A. These effects along with hot-carrier degradation discussed in [87] should be considered in optimizing the film thickness for high performance VLSI circuits.

The quality of the buried oxide could have an important effect on the statistical variation of the threshold voltage of an SOI MOSFET. Any nonuniform charge distribution in the buried oxide can contribute extra instability to the threshold voltage. For a near-intrinsic thin-film SOI MOSFET, the charge in the buried oxide could be greater than the depletion-region areal charge Q_b. Therefore, the statistical distribution of the threshold voltage could be dominated by the charge in the buried oxide rather than the depletion-region areal charge. There are two approaches to reduce the influence of the charge in the buried oxide [95] : (i) a negative back gate bias could be used to eliminate the sensitivity of threshold voltage on this charge; (ii) reduction of front or back gate oxide thickness. However, the most practical solution to this problem is to reduce the charge in the buried oxide by improving the SIMOX technology.

6.5 Conclusion

In conclusion, we have analyzed and compared the statistical variation effects in both the bulk and SOI MOSFET's. The maximum allowable doping concentration and the film thickness for reduced threshold voltage distribution in the SOI MOSFET's are discussed. Based on our simulations, we have shown the inherent advantage of the SOI MOSFETs over their bulk silicon counterparts with regard to the statistical variation of the threshold voltage. The simulation presented in this Chapter did not consider the effect of the charge in the buried oxide. The importance of this charge could be detrimental if it is not well controlled. With continuous progress in the SIMOX technology, this charge could be reduced in its density and the yield of the SOI circuit could be as good as or better than its bulk silicon counterpart.

Table 6.1 Nominal device parameters used in the statistical analysis.

Parameter	Mean μ	Standard Deviation σ
N_a	10^{16} cm^{-3}	5×10^{14} cm^{-3}
t_{ox}	25 nm	2 nm
t_b	0.20 μm	10 nm
t_{ob}	0.35 μm	–
L	> 10 μm	0.1 μm
T	300 K	10 K

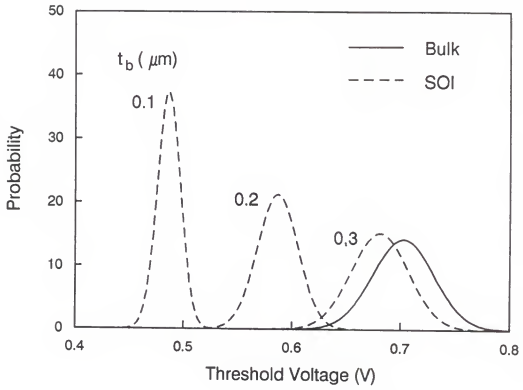

Figure 6.1 Probability distribution of the threshold voltage, with film thickness t_b as a parameter, calculated by considering a Gaussian distribution of gate oxide thickness t_{ox} with a standard deviation $\sigma(t_{ox})$ of 2 nm. Other device parameters are kept constant as shown in Table 6.1.

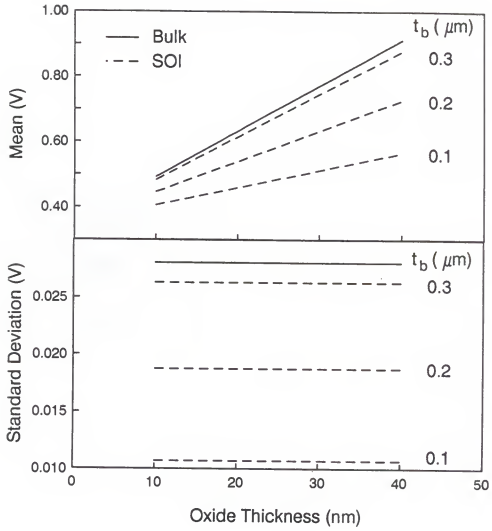

Figure 6.2 Mean value and standard deviation of the threshold voltage as a function of gate oxide thickness t_{ox} for different film thicknesses t_b. A standard deviation $\sigma(t_{ox})$ of 2 nm is assumed.

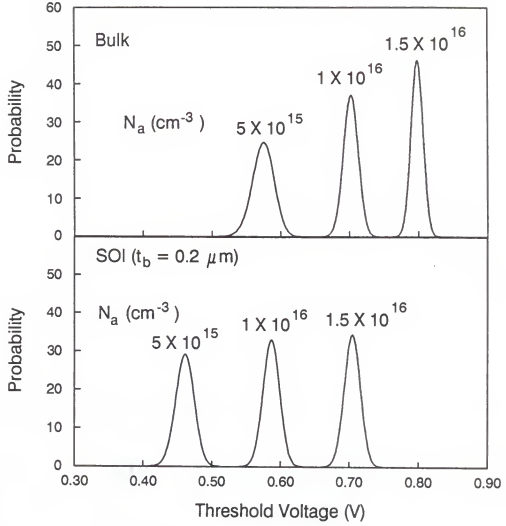

Figure 6.3 Probability distribution of the threshold voltage for three values of channel doping concentrations N_a, calculated by considering a Gaussian distribution of doping concentration with a standard deviation $\sigma(N_a)$ of 5×10^{14} cm^{-3}.

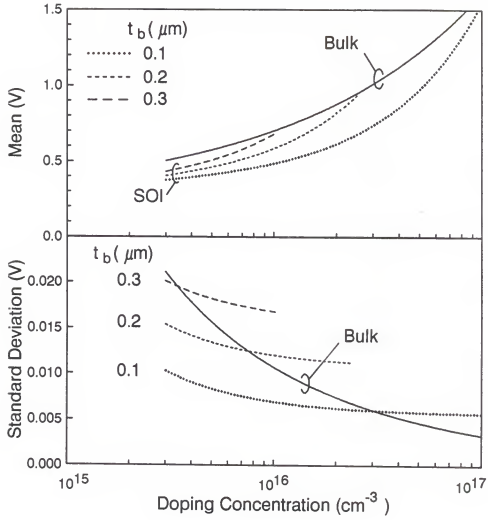

Figure 6.4 Mean value and standard deviation of the threshold voltage as a function of doping concentration N_a for different film thicknesses. A standard deviation $\sigma(N_a)$ of 5×10^{14} cm^{-3} is assumed.

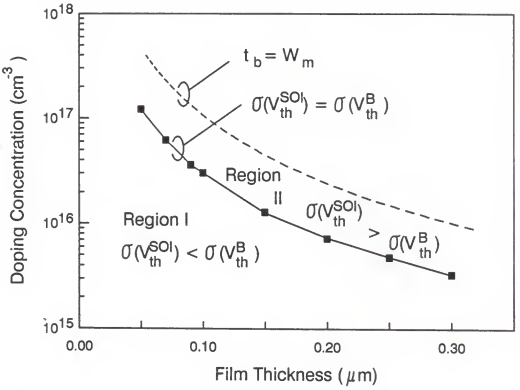

Figure 6.5 Contour plot of the standard deviation of the threshold voltage $\sigma(V_{th})$. The solid line is determined by $\sigma(V_{th}^{SOI}) = \sigma(V_{th}^{B})$. The dashed line is the constrain imposed by the requirement of a fully depleted film.

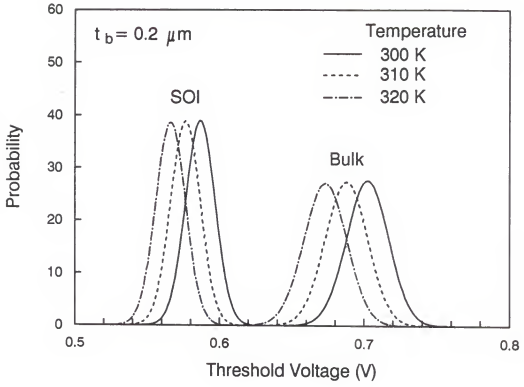

Figure 6.6 Probability distribution of the threshold voltage reduction for three values of channel lengths L, calculated by considering a Gaussian distribution of channel length with a standard deviation σ(L) of 0.1 μm.

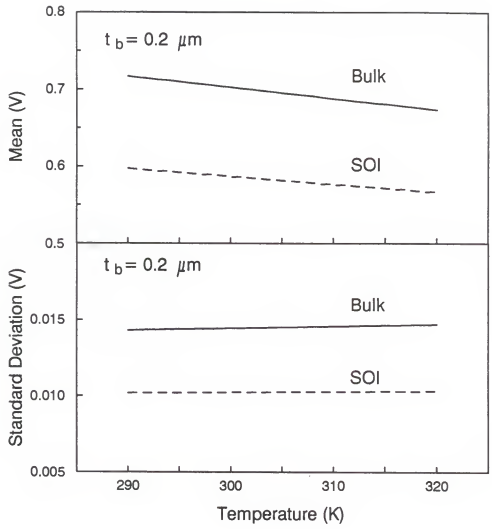

Figure 6.7 Mean value and standard deviation of the threshold voltage reduction as a function of channel length L with different film thicknesses t_b as a parameter. A standard deviation σ(L) of 0.1 μm is assumed.

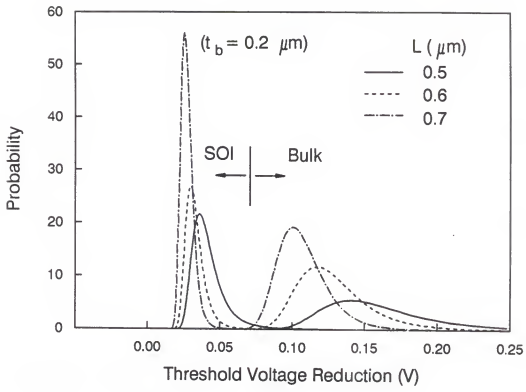

Figure 6.8 Probability distribution of the threshold voltage for different film thicknesses t_b, calculated by considering a Gaussian distribution of film thickness with a standard deviation $\sigma(t_b)$ of 10 nm.

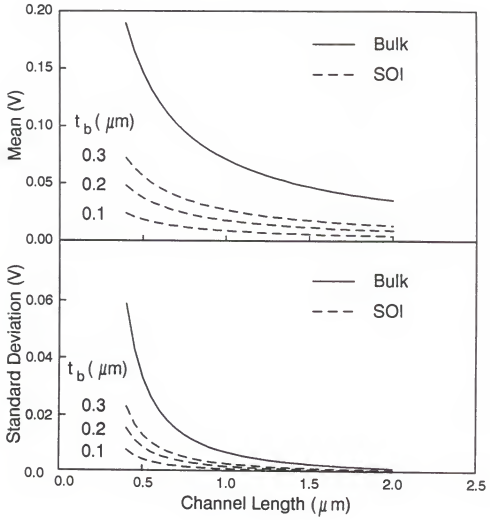

Figure 6.9 Mean value and standard deviation of the threshold voltage as a function of film thickness t_b. A standard deviation $\sigma(t_b)$ of 10 nm is assumed.

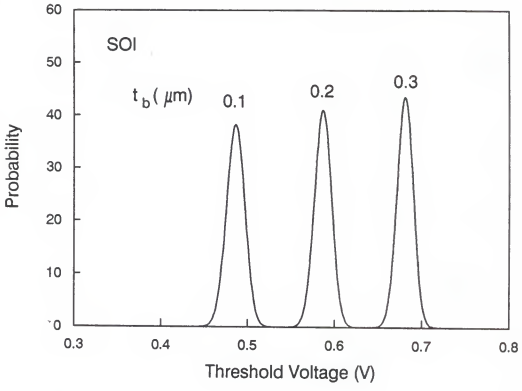

Figure 6.10 Probability distribution of the threshold voltage for three operation temperatures T, calculated by considering a Gaussian distribution of temperature with a standard deviation σ(T) of 10 K. A film thickness t_b of 0.2 μm is assumed.

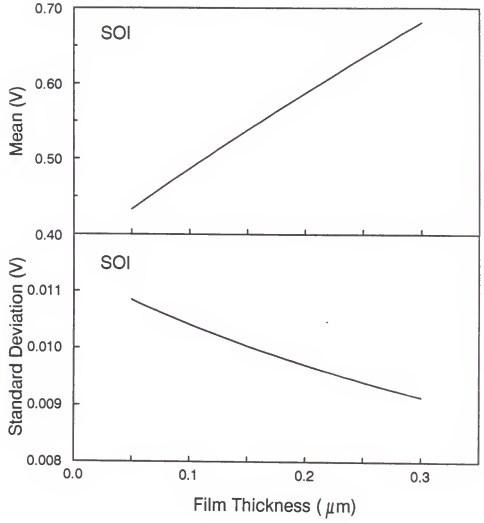

Figure 6.11 Mean value and standard deviation of the threshold voltage as a function of temperature T. A standard deviation σ(T) of 10 K and a film thickness t_b of 0.2 μm is assumed.

CHAPTER 7
SUMMARY AND CONCLUSIONS

This work deals with the modeling of SOI devices for material and device characterization, and the design considerations for future VLSI circuit manufacturability. It consists of two parts. The first part develops several electrical characterization techniques using test structures such as diode, capacitor, and MOSFET for evaluating the film and the interface properties of the SOI materials and devices. The second part discusses on the design considerations for VLSI circuit manufacturability in SOI MOSFET's.

The thin silicon film on the SOI substrate often has properties that vary with distance from the top surface of the film to the film/buried oxide interface. The generation lifetime profile in thin silicon film grown on the SIMOX substrate enables us to assess the role of oxygen implantation and post implantation annealing on the introduction of generation-recombination centers and their effect on device performance. A differential technique for evaluating the generation lifetime profile and interface generation velocity in thin semiconductor films has been developed. The results suggest that deep-level defects in the silicon film is an important factor which can influence the film quality. However, as the film thickness is greatly reduced and the oxygen implantation process is constantly improved, the buried oxide interface properties become an important factor in determining the device performance.

The MOS capacitor theory for characterizing the bulk and interface properties has been well established since early 1970's. This theory plays a very important role in the development of MOS technology for current VLSI applications. Due to the unique configuration of SOI substrate, the MOS theory cannot be directly applied

to the SOI substrate. The SIS capacitor is a natural candidate for evaluating both buried oxide interfaces and film properties of the SOI substrate. A model has been developed for electrical characterization of the interface properties in a SIS capacitor using capacitance and conductance methods. By introducing a coupling factor, conventional MOS capacitor theory is modified and applies to analyze the properties of the film/oxide and the substrate/oxide interfaces of a SIS capacitor. The model enabled us to extract doping concentration, buried oxide thickness, fixed oxide charge, and interface state density from the static and dynamic capacitance and conductance measurements on a simple SIS capacitor formed on the SIMOX substrates.

Several transient capacitance techniques are also being modified for the characterization of the SIS capacitor which include Zerbst, temperature-scan DLTS, and bias-scan DLTS techniques. By appropriate pulsing the SIS capacitor, the charge coupling between the film and the substrate can be neglected without introducing significant error. Therefore, Zerbst and temperature-scan DLTS techniques can be applied to the SIS capacitor without modification. Bias-scan DLTS involves scanning the gate bias while applying small filling pulses at constant temperature. Using this technique we have determined interface state densities and capture cross sections of SIMOX based SIS capacitors at both the film/oxide and the substrate/oxide interfaces. Also, methods of distinguishing among different sources of transient signals such as bulk traps, interface states, and minority carrier generation are discussed.

Characterization of interface states in small geometry MOSFET's is a subject of intensive research in recent years. Due to the very small gate area of VLSI MOSFET's, conventional capacitance and conductance methods are not possible for characterization of interface states. The transconductance is sensitive to the interface states and fixed oxide charges, and is frequently used to monitor the effect of hot-carrier stress and accelerated aging on device reliability. Transconductance techniques for the characterization of interface states in small geometry MOSFET's operating in the

linear region have been developed. In fact, the ideal is very interesting since it implies that the small signal transistor current can furnish the same information about the interface states as the small signal capacitor currents which is several orders of magnitude lower due to the very small gate area.

The strengths and weaknesses of the proposed characterization methods are summarized in Tables 7.1 and 7.2. For characterizing the bulk properties, we suggest the current-capacitance technique, since this method provides a self-consistent check which ensures the accuracy of the experimental results. For interface characterization, combined high-low frequency capacitance method is suggested due to its simplicity of experimental procedure. However, with the aid of automated computer acquisition system, conductance method would provide more accurate result. For ultra-thin film SOI material, transconductance method is believed to be a better candidate. Although charge-pumping technique is widely accepted in bulk MOSFET's, the lack of body contact in SOI MOSFET's may impose some limitation. Even if the body contact exists, the large series resistance of thin silicon film would impose severe constrains on the charge-pumping measurement.

Design considerations for yield enhancement of VLSI circuits on SOI substrate is investigated by examining the statistical variation of threshold voltage induced by random distributed device parameters. The analysis reveals that thin-film SOI MOSFET's is less sensitive to inherent fluctuations in device parameters. By proper choosing the gate material, film thickness, and the channel doping density, enhancement of production yield can be expected for high performance SOI VLSI circuits.

Because of its many compelling advantages in radiation and harsh environments, SOI technology is very attractive for military ICs. As a consequence, SOI will probably be employed initially in radiation and space applications. It is also likely that SOI technology will become important for submicron devices. In many instances, SOI is the only viable solution to the technology problems introduced by continued

scaling of device feature size in CMOS/VLSI applications. Being "transparent" to bulk silicon process lines, SIMOX will be subjected to the same learning-curve process that drives the cost of IC manufacturing. Although, SIMOX material quality is still inferior to bulk silicon material, an increasing body of evidence is showing that yield on SIMOX based 64K SRAMS is as good as or better than what they would achieve with the same circuit on bulk silicon material [92]. It is expected that if the trends continue, the SIMOX technology will be utilized in commercial as well as military applications in an effort to maintain the current rate of scaling to smaller feature sizes and higher density. As a consequence, the cost of a SIMOX wafer will decrease as volume increases and that the cost will be competitive with that of an epitaxial wafer.

Table 7.1 Summary of strengths and weaknesses of different characterization techniques for determining the silicon film properties.

Techniques	Structure	Strengths	Weaknesses
Lifetime Profile	Diode	Simple I-V & C-V, Nonuniform N_d	
Zerbst Method	SISC	Simple C-t Measurement	Uniform N_d
Conventional DLTS	SISC	Detail Defect Parameters	Temperature Variation

Table 7.2 Summary of strengths and weaknesses of different characterization techniques for determining the Si/SiO_2 interface properties.

Techniques	Structure	Strengths	Weaknesses
Gated Diode	Diode, MOSFET	Simple I-V Measurement	Averaged D_{it}
Conventional DLTS	SISC	Identify D_{it} or N_t	Temperature Variation
Bias Scan DLTS	SISC	No Temp. Variation	Limited Energy Resolution
C-V	SISC	Simple C-V Measurement	Less Sensitive
G-ω	SISC	Higher Sensitivity	Limited Energy Range
g_m-V	MOSFET	Simple g_m Measurement	Less Sensitive
g_m-ω	MOSFET	Higher Sensitivity	Limited Energy Range
I_{cp}-ω	MOSFET	High Sensitivity	Averaged D_{it}, Series Resistance

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BIOGRAPHICAL SKETCH

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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Sheng S. Li, Chairman
Professor of Electrical Engineering

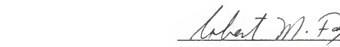
I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Dorothea E. Burk
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Gÿs Bosman
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.



Robert M. Fox
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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

May 1991

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